S J P N Trust's

Hirasugar Institute of Technology, Nidasoshi

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Department of Electrical & Electronics Engineering

Electronics Laboratory

Manual

18EEL38

Lab Incharge

Prof. A. U. Neshti & Prof. S. S. Birade

Lab Instructor

Shri. V. M. Mutalik

AY 2021-22

Department of Electrical & Electronics Engineering

VISION

To be the centre of excellence in teaching and learning to produce the competent & socially responsible professionals in the domain of Electrical & Electronics Engineering.

MISSION

To educate students with core knowledge of Electrical & Electronics Engineering by developing problem solving skills, professional skills and social awareness to excel in their career.

Overview

Year / Semester	2nd Year /3rd Semester		**Academic Year**	2021 - 22
Laboratory Title	Electronics Lab		**Laboratory Code**	18EEL38
Total Contact Hours	42 Hours		**Duration of SEE**	3 Hours
CIE Marks	40 Marks		**SEE Marks**	60 Marks
Lab Manual Author	Prof. Sagar S Birade	**Sign -**	**Date**	**30-09-2021**
Checked By		**Sign -**	**Date**	

Objectives

- To design and test half wave and full wave rectifier circuits.
- To design and test different amplifier and oscillator circuits using BJT.
- To study the simplification of Boolean expressions using logic gates.
- To realize different Adder and Subtractor circuits.
- To design and test counters and sequence generators.

Description

1.0 Learning Objectives

Student aims to understand, design and analyze the basic applications of the diodes, transistors, logic gates and various IC's. In this laboratory student designs many circuits' namely rectifiers, transistor amplifiers, RC phase shift oscillator, realize adder/subtractor circuit, code conversion and counter circuits etc.

2.0 Learning Outcomes

The student, after successful completion of the course, will be able to

1. To design and test half wave and full wave rectifier circuits.
2. To design and test different amplifier and oscillator circuits using BJT.
3. To study the simplification of Boolean expressions using logic gates.
4. To realize different Adders and Subtractors circuits.
5. To design and test counters and sequence generators.

Prerequisites

- Basic knowledge of bread board connection methods.
- Details of various elements like pin configuration of different logic gates, color code of resistors etc.
- Analog Electronic Circuits design and analysis

Base Course

1. Analog Electronic Circuits.
2. Basic Electrical/Electronics Engineering.

Introduction

In Electronics Lab we are conducting experiments such as rectifiers, transistor amplifiers, RC phase shift oscillator, realize adder/subtractor circuit, code conversion and counter circuits etc using Diode, Transistors, Logic Gates and various IC's. At the end of the course student will be able to understand and design transistor circuits, digital circuits and get the performance practically.

Resources Required

1. Signal Generator
2. Regulated Power Supply
3. Digital Storage Oscilloscope
4. Bread Boards

General Instructions

1. After circuit connection, before switching ON the supply, verify it by instructor/ lab in charge.
2. Make sure voltage level of power supply is at minimum value at the start.
3. Before leaving the lab keep all the equipments properly.

Contents

Expt No.	Title of the Experiment	Date Planned	Date Conducted
1	Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency.		
2	Static Transistor characteristics for CE, CB and CC modes and determination of h parameters.		
3	Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.		
4	Design and testing of BJT - RC phase shift oscillator for given frequency of oscillation.		
5	Determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping.		
6	Simplification, realization of Boolean expressions using logic gates/Universal gates.		
7	Realization of half/Full adder and Half/Full Subtractors using logic gates.		
8	Realization of parallel adder/Subtractors using 7483 chip- BCD to Excess-3 code conversion & Vice -Versa.		
9	Realization of Binary to Gray code conversion and vice versa.		
10	Design and testing Ring counter/Johnson counter.		
11	Design and testing of Sequence generator.		
12	Realization of 3 bit counters as a sequential circuit and MOD – N counter design using 7476, 7490, 74192, 74193.		

Evaluation Scheme

1. Lab activity – Continuous Assessment, Attendance, Journal – 24 Marks.
2. Internal exam at the end of semester – 16 Marks.
3. Semester End Exam – 100 Marks (scaled down to 60).

Reference

1. 'Electronic Devices and Circuit Theory', Robert L Boylestad Louis Nashelsky Published by Pearson 11th Edition 2015.
2. Fundamentals of Analog Circuits Thomas L Floyd Pearson 2nd Edition, 2012.
3. "Digital Integrated Electronics" by H. Taub and D. Schilling
4. https://www.aec.at/futurelab/en/

EXPERIMENT NO -1
Full Wave and Bridge Rectifiers

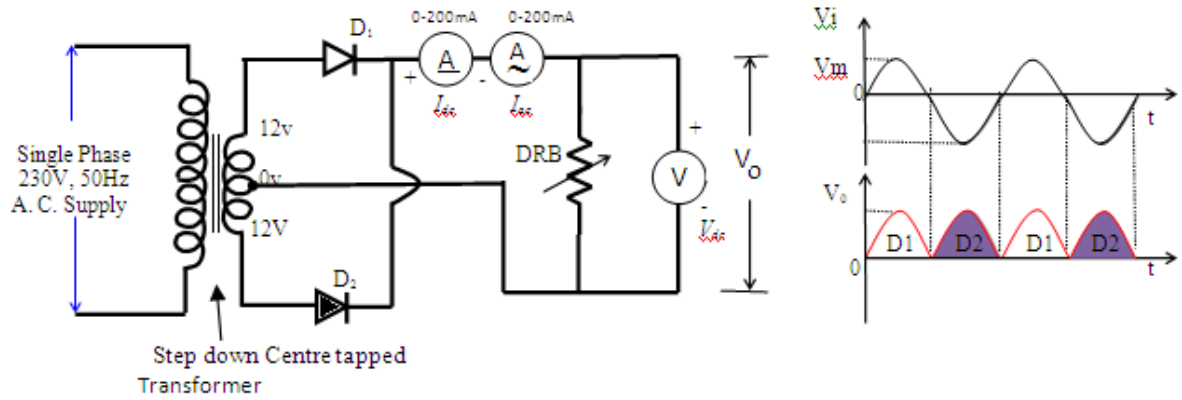
Aim: Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency

Apparatus Required:

Sl. No	Name of the Component	Type	Range	Quantity
1	Bread Board	-	-	1
2	Diode	-	1N4007	4
3	Centre tapped transformer	-	12-0-12V	1
4	Ammeter	Digital	0-200mA AC&DC	1 each
5	Voltmeter	Analog	0-30V DC	1
6	Capacitor	Electrolyte	470µF/25V	1
7	Connecting Wire	Single strand	-	few

Full Wave rectifier without Filter

Circuit Diagram:



Design:

Choosing transformer with secondary voltage V_s= 12V

From the data sheet we have, $I_{L\,(max)}$ = 150mA

For Full Wave rectifier $V_{dc} = \frac{2Vm}{\pi}$ = 10.8V

$$R_L = \frac{V_{dc}}{I_{L(Max)}} = \frac{10}{150m} = 10.8/150m = 72\ \Omega\ [\text{ Std } 100\ \Omega]$$

Power dissipated in R_L is

$$P_L = V_{dc} \times I_{L(max)} = 10.8 \times 150 \times 10^{-3} = 1.5 \text{ watts}$$

Choose R_L = 100Ω with the help of DRB

Calculations:

Ripple factor $\gamma = \frac{I_{ac}}{I_{dc}}$

% Efficiency $\eta = \frac{I^2_{dc}}{I^2_{dc} + I^2_{ac}}$ x 100

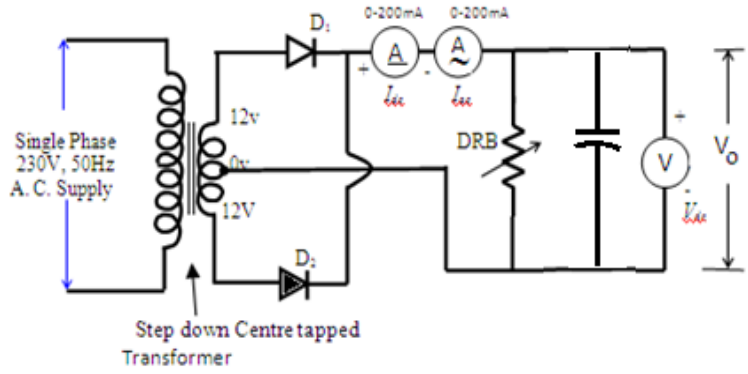
% Regulation = $\frac{V_{dc\,(NL)} - V_{dc}}{V_{dc}}$ x 100

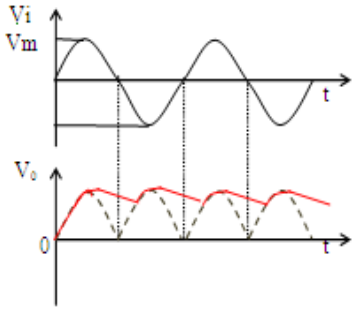
Tabular Column:

R_L in Ω	V_{dc} in volts	I_{dc} in mA	I_{ac} in mA	Ripple factor (γ)	Efficiency	% Regulation
Max (NL)						

Full Wave rectifier with C- Filter

Circuit Diagram





Design:

To design a Full wave rectifier with C-filter for the following specifications

Choosing transformer with secondary voltage V_s= 12V, $I_{L(max)}$ = 150mA and ripple factor =0.04

For Full Wave rectifier with C-filter V_{dc} =17V

$$R_L = \frac{V_{dc}}{I_{L(Max)}} = \frac{17}{150m} = 113.13\Omega \text{ [Std 150 } \Omega\text{]}$$

Power dissipated in R_L is

$$P_L = V_{dc} \times I_{L(max)} = 17 \times 150 \times 10^{-3} = 2.55 \text{ watts}$$

Choose R_L = 150Ω [use DRB]

For Full wave rectifier with C-filter

$$\text{Ripple factor} = \frac{1}{4\sqrt{3}\, f R_L C}$$

Therefore $$C = \frac{1}{4\sqrt{3} \times 50 \times 150 \times 0.04} = 481\ \mu F$$

Choose C= 470 µF /25V a standard value

Calculations:

$$\text{Ripple factor } \gamma = \frac{I_{ac}}{I_{dc}}$$

Tabular column:

R_L in Ω	I_{dc} in mA	I_{ac} in mA	Ripple factor (γ)

Procedure:

For Full Wave Rectifier

1. Connect the circuit as shown in figure.
2. Set the DRB to maximum and note down value of V_{dc} (No Load) (here maximum resistance is designated as No load).
3. Vary the DRB (in steps of 100Ω, 200Ω, 300Ω) and note down the values of I_{dc}, I_{ac}, and V_{dc} and record the readings in the tabular column.
4. Observe the output waveforms on the Oscilloscope and draw these waveforms to scale.
5. For each value of I_{dc} determine the values of ripple factor, efficiency and regulation.

6. Connect the circuit with Capacitor -filter as shown in the fig 4.
7. Calculate the value of Capacitor for the given value of ripple factor (Assume R_L to some value) by using the formula and then repeats the steps 2-5

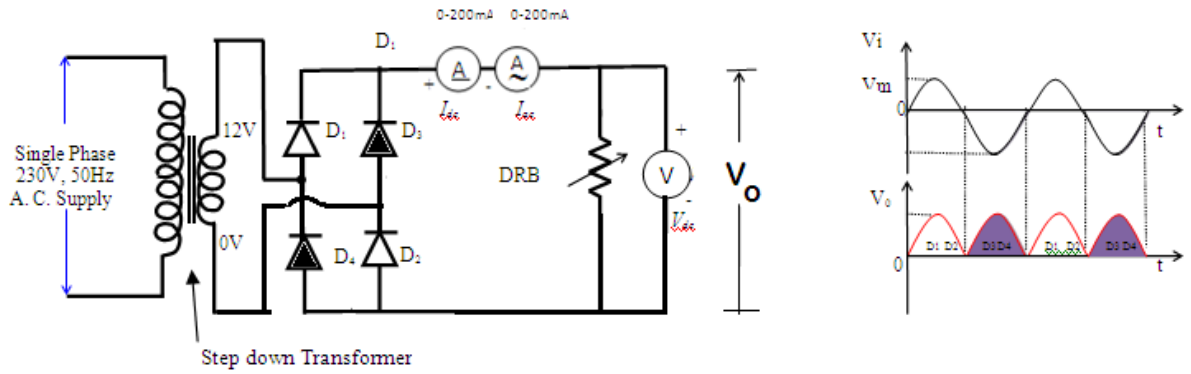
Result:

	Ripple Factor	Efficiency	% Regulation
Full wave Bridge rectifier without Filter			
Full wave Bridge rectifier with C-Filter			

Conclusion:

Full Wave Bridge Rectifier without Filter

Circuit Diagram:



DESIGN:

Choosing transformer with secondary voltage V_s= 12V, $I_{L(max)}$ = 150mA

For Full Wave Rectifier $V_{dc} = \frac{2Vm}{\pi}$ = 10.8V

$$R_L = \frac{V_{dc}}{I_{L(Max)}} = 10.8/150m = 72\ \Omega\ [\text{Std } 100\ \Omega]$$

Power dissipated in R_L is

$$P_L = V_{dc} \times I_{L(max)} = 10.8 \times 150 \times 10^{-3} = 1.5 \text{ watts}$$

Choose $R_L = 100\Omega$ [use DRB]

Calculations:

Ripple factor $\gamma = \frac{I_{ac}}{I_{dc}}$

%Efficiency $\eta = \frac{I^2_{dc}}{I^2_{dc} + I^2_{ac}} \times 100$

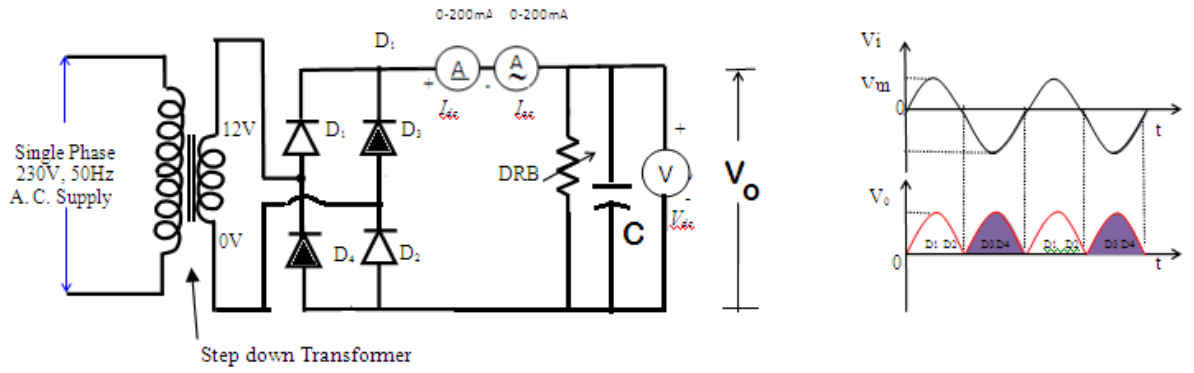
% Regulation $= \frac{V_{dc\,(NL)} - V_{dc}}{V_{dc}} \times 100$

Tabular column:

R_L in Ω	V_{dc} in volts	I_{dc} in mA	I_{ac} in mA	Ripple Factor (γ)	Efficiency	%Regulation
Max (NL)						

Full Wave Bridge Rectifier with C- Filter

Circuit Diagram:



Design:

Choosing transformer with secondary voltage V_s= 12V, $I_{L(max)}$ = 150mA and ripple factor =0.04

For Full Wave rectifier with C-filter V_{dc} = 17V

Power dissipated in R_L is

$$P_L = V_{dc} \times I_{L(max)} = 17 \times 150 \times 10^{-3} = 2.55 \text{ watts}$$

Choose R_L = 150Ω [use DRB]

For Full wave rectifier with C-filter Ripple factor $= \frac{1}{4\sqrt{3}\, f R_L C}$

Therefore $C = \frac{1}{4\sqrt{3} \times 50 \times 150 \times 0.04}$ = 481 µF [Choose C= 470 µF /25V a standard value]

Calculations:

$$\text{Ripple factor } \gamma = \frac{I_{ac}}{I_{dc}}$$

Tabular column:

R_L in Ω	I_{dc} in mA	I_{ac} in mA	Ripple factor (γ)

Procedure:

For Full Wave Bridge Rectifier

1. Connect the circuit as shown in circuit diagram.5
2. Set the DRB to maximum and note down value of V_{dc} (No Load) (here maximum resistance is designated as No load).
3. Vary the DRB (in steps of 100Ω, 150Ω, 300Ω)and note down the values of I_{dc}, I_{ac}, and V_{dc} and record the readings in the tabular column.
4. Observe the output waveforms on the Oscilloscope and draw these waveforms to scale.
5. For each value of I_{dc} determine the values of ripple factor, efficiency and regulation.

6. Connect the circuit with Capacitor -filter as shown in the fig 6.
7. Calculate the value of Capacitor for the given value of ripple factor (Assume R_L to some value) by using the formula and then repeats the steps 2-5

Result:

	Ripple Factor	Efficiency	% Regulation
Full wave Bridge rectifier without Filter			
Full wave Bridge rectifier with C-Filter			

CONCLUSION:

Experiment No. 2

CE, CB & CC CONFIGURATIONS

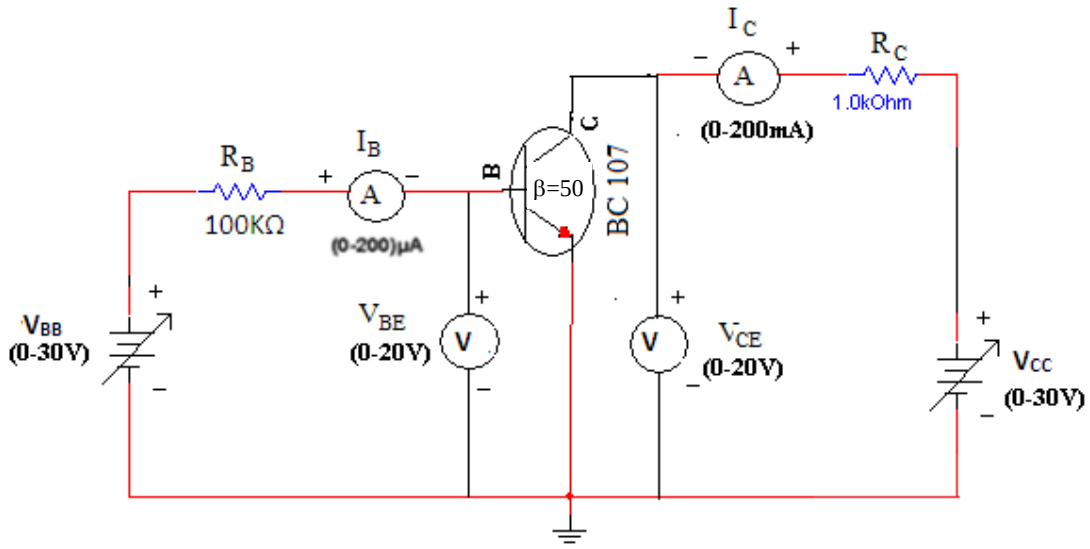
Common Emitter Configuration

Aim: To study the input and output characteristics of a transistor in Common Emitter configuration.

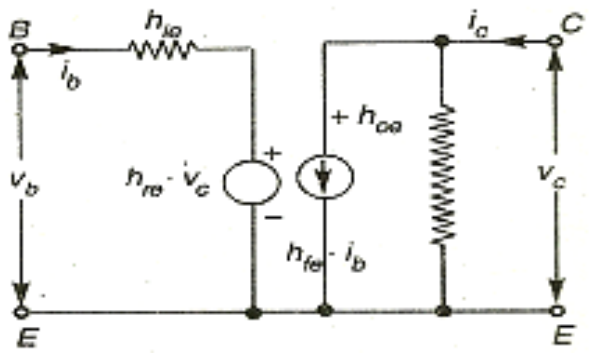
Apparatus Required:

Sl. No.	Name	Type	Range	Quantity
1	Transistor	npn	BC107	1 No.
2	Resistors	-	1KΩ,100KΩ	1 No. Each
3	Bread board	-		1 No.
4	Dual Regulated Power supply	DC	0-30 V/2A	1 No.
5	Ammeters	Digital	0 - 200 mA, 0-200 μA	1 No. Each
6	Voltmeter	Digital	0 - 20V	2 No.
7	Connecting wires	Single Strand	-	Few.

Circuit Diagram:



h – Parameter model of CE transistor:

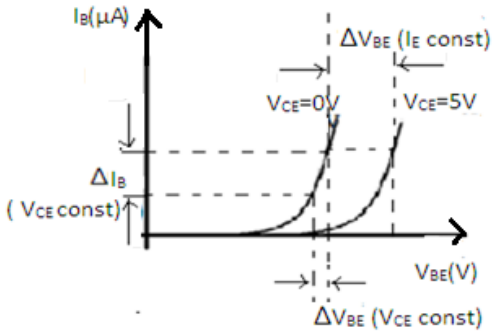


Observations:

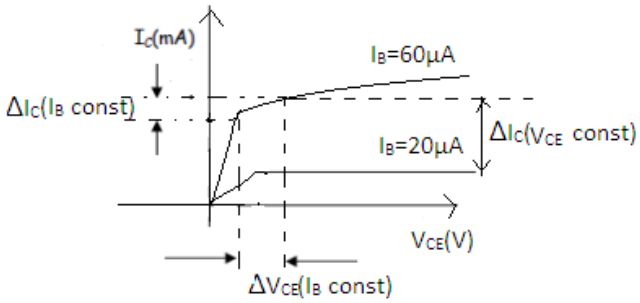
Input Characteristics				
V_{BB} (Volts)	V_{CE} = 0V		V_{CE} = 5V	
	V_{BE} (Volts)	I_B (µA)	V_{BE} (Volts)	I_B (µA)

Output Characteristics						
V_{CC} (Volts)	I_B = 0 µA		I_B = 20 µA		I_B = 40 µA	
	V_{CE} (Volts)	I_C (mA)	V_{CE} (Volts)	I_C (mA)	V_{CE} (Volts)	I_C (mA)

Graph:



Input Characteristics



Output Characteristics

Procedure:

Input Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage V_{CE} = 0V by varying V_{CC}.
3. Varying V_{BB} gradually, note down base current I_B and base-emitter voltage V_{BE}.
4. Step size is not fixed because of non linear curve. Initially vary V_{BB} in steps of 0.1V. Once the current starts increasing vary V_{BB} in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for V_{CE} = 5V.

Output Characteristics:

1. Connect the circuit as shown in the circuit diagram.

2. Keep emitter current $I_B = 20\mu A$ by varying V_{BB}.
3. Varying V_{CC} gradually in steps of 1V up to 12V and note down collector current I_C and Collector-Emitter Voltage (V_{CE}).
4. Repeat above procedure (step 3) for $I_B = 60\mu A, 0\mu A$.

To Plot Graph:

1. Plot the input characteristics by taking V_{BE} on X-axis and I_B on Y-axis at a constant V_{CE} as a constant parameter.
2. Plot the output characteristics by taking V_{CE} on X-axis and taking I_C on Y-axis taking I_B as a constant parameter.

Calculations from Graph:

1. Input Characteristics: To obtain input resistance find ΔV_{BE} and ΔI_B for a constant V_{CE} on one of the input characteristics.
   Input impedance $h_{ie} = R_i = \Delta V_{BE} / \Delta I_B$ (V_{CE} is constant)
   Reverse voltage gain $h_{re} = \Delta V_{EB} / \Delta V_{CE}$ (I_B = constant)
2. Output Characteristics: To obtain output resistance find ΔI_C and ΔV_{CB} at a constant I_B.
   Output admittance $1/hoe = R_o = \Delta I_C / \Delta V_{CE}$ (I_B is constant)
   Forward current gain $hfe = \Delta I_C / \Delta I_B$ (V_{CE} = constant)

Result:

The h-parameters for a transistor in CE configuration are:

a. The Input Resistance (h_{ie}) _____Ohms.
b. The Reverse Voltage Gain (h_{re}) _____.
c. The Output Conductance (h_{oe}) _____ Mhos.
d. The Forward Current Gain (h_{fe}) _____.

Conclusion:

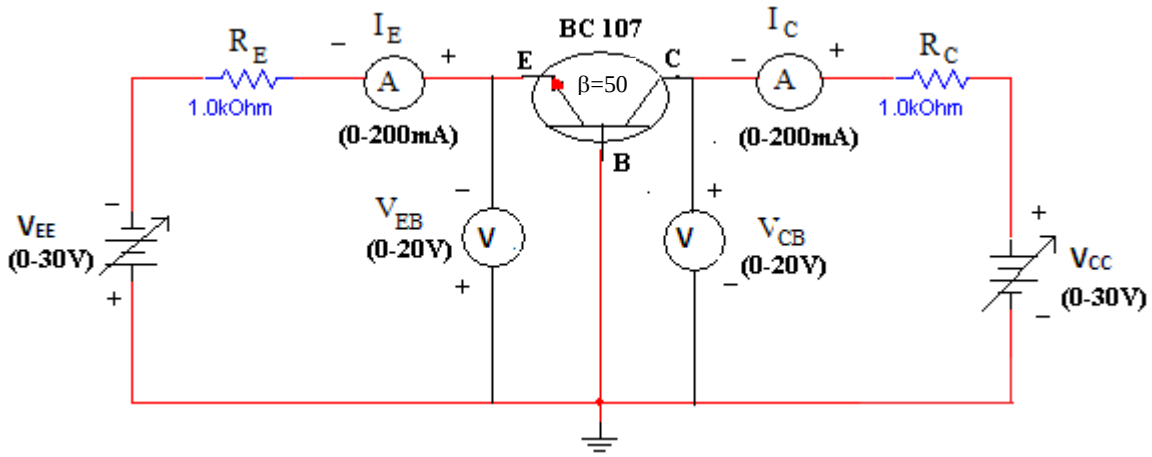
Common Base Configuration

Aim: To study the input and output characteristics of a transistor in Common Base Configuration.

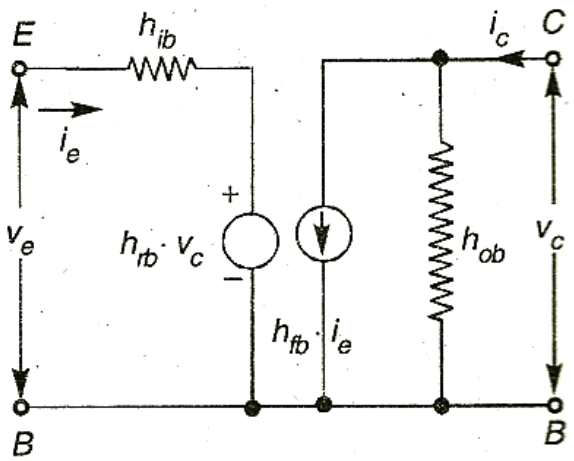
Apparatus Required:

Sl. No.	Name	Type	Range	Quantity
1	Transistor	npn	BC107	1 No.
2	Resistors	-	1KΩ	2 No.s
3	Bread board	-	-	1 No.
4	Dual Regulated Power supply	DC	0-30 V/2A	1 No.
5	Ammeters	Digital	0 - 200 mA, 0-200mA	1 No. Each
6	Voltmeter	Digital	0 - 20V	2 No.
7	Connecting wires	Single Strand	-	Few.

Circuit Diagram:



h – Parameter model of CB transistor:

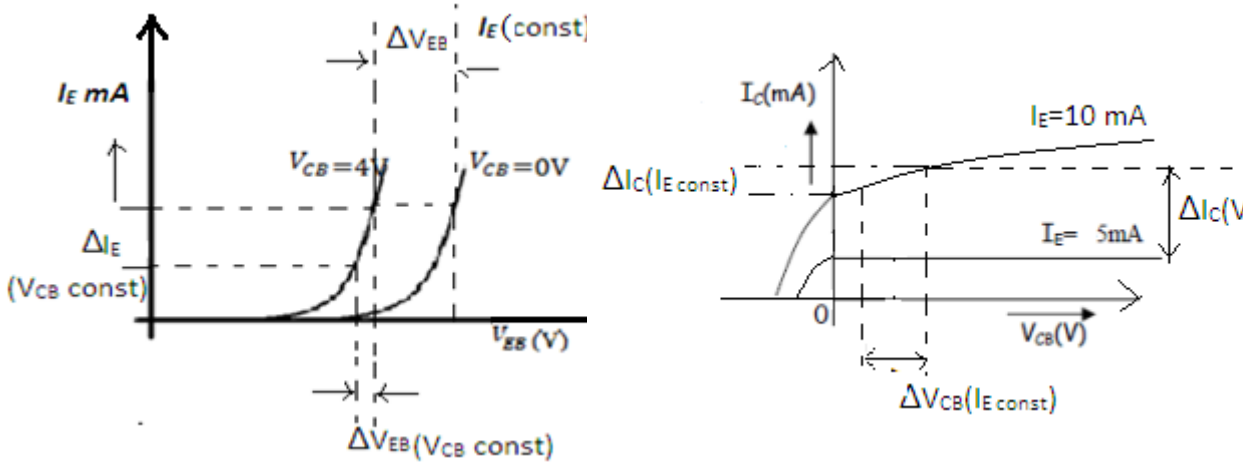


Observations:

Input Characteristics				
V_{EE} (Volts)	V_{CB} = 0V		V_{CB} = 4V	
	V_{EB} (Volts)	I_E (mA)	V_{EB} (Volts)	I_E (mA)

Output Characteristics						
V_{CC} (Volts)	I_E = 0mA		I_E = 5V		IE = 10mA	
	V_{CB} (Volts)	I_C (mA)	V_{CB} (Volts)	I_C (mA)	V_{CB} (Volts)	I_C (mA)

Graph:



1. Plot the input characteristics for different values of $\mathbf{V_{CB}}$ by taking $\mathbf{V_{EE}}$ on X-axis and $\mathbf{I_E}$ on Y-axis taking $\mathbf{V_{CB}}$ as constant parameter.
2. Plot the output characteristics by taking $\mathbf{V_{CB}}$ on X-axis and taking $\mathbf{I_C}$ on Y-axis taking $\mathbf{I_E}$ as a constant parameter.

Procedure:

Input Characteristics:

1) Connect the circuit as shown in the circuit diagram.
2) Keep output voltage V_{CB} = 0V by varying V_{CC}.
3) Varying V_{EE} gradually, note down emitter current I_E and emitter-base voltage(V_{EE}).
4) Step size is not fixed because of nonlinear curve. Initially vary V_{EE} in steps of 0.1 V. Once the current starts increasing vary V_{EE} in steps of 1V up to 12V.
5) Repeat above procedure (step 3) for V_{CB} = 4V.

Output Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep emitter current I_E = 5mA by varying V_{EE}.
3. Varying V_{CC} gradually in steps of 1V up to 12V and note down collector current I_C and collector-base voltage (V_{CB}).
4. Repeat above procedure (step 3) for I_E = 10mA.
5.

Repeat above procedure (step 3) for I_E = 10mA.

Calculations from Graph:

The h-parameters are to be calculated from the following formulae:

1. **Input Characteristics:** To obtain input resistance, find ΔV_{EE} and ΔI_E for a constant V_{CB} on one of the input characteristics.

   Input impedance $h_{ib} = R_i = \Delta V_{EE} / \Delta I_E$ (V_{CB} = constant)
   Reverse voltage gain $hrb = \Delta V_{EB} / \Delta V_{CB}$ (I_E = constant)
2. **Output Characteristics:** To obtain output resistance, find ΔI_C and ΔV_{CB} at a constant I_E.

   Output admittance $h_{ob} = 1/Ro = \Delta I_C / \Delta V_{CB}$ (I_E = constant)
   Forward current gain $h_{fb} = \Delta I_C / \Delta I_E$ (V_{CB} = constant)

Result:

The h-parameters for a transistor in CB configuration are:

a. The Input resistance (h_{ib}) _____ Ohms.
b. The Reverse Voltage Transfer Ratio (h_{rb}) _____.
c. The Output Admittance (h_{ob}) _____ Mhos.
d. The Forward Current gain (h_{fb}) _____.

Conclusion:

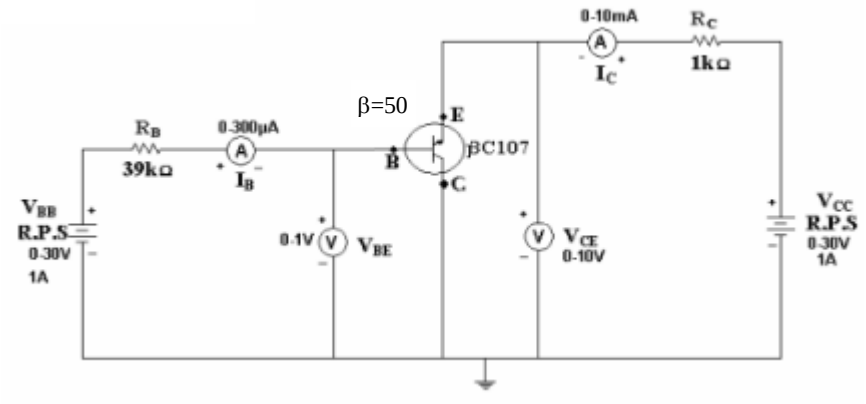
Common Collector Configuration

Aim: To study the input and output characteristics of a transistor in Common Collector Configuration.

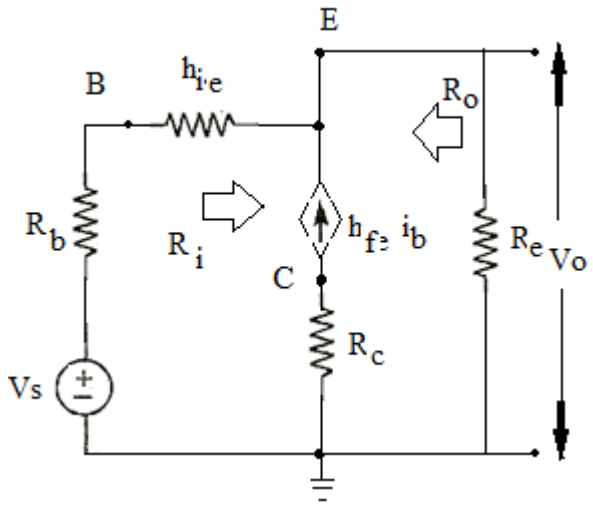
Apparatus Required:

Sl. No.	Name	Type	Range	Quantity
1	Transistor	npn	BC107	1 No.
2	Resistors	-	39KΩ,1KΩ	1 No. Each
3	Bread board	-	-	1 No.
4	Dual Regulated Power supply	DC	0-30 V/2A	1 No.
5	Ammeters	Digital	0 - 200mA, 0-200μA	1 No. Each
6	Voltmeter	Digital	0 - 20V	2 No.
7	Connecting wires	Single Strand	-	Few.

Circuit Diagram:



h – Parameter model of CB transistor:

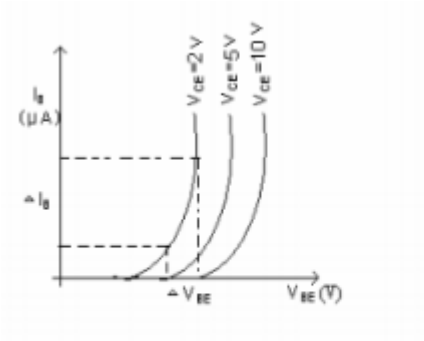


Observations:

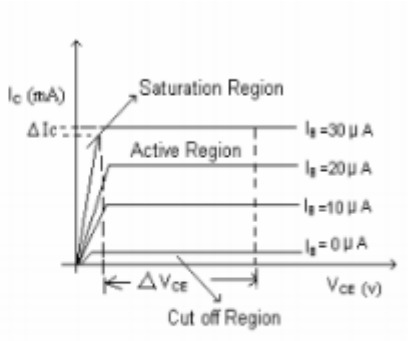
Input Characteristics							
Sl. No	Applied Voltage V_{BB} (V)	V_{CE} = 2V		V_{CE} = 5V		V_{CE} = 10V	
		V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)	V_{BE} (V)	I_B (µA)
1							
2							
3							
4							
5							

Output Characteristics							
Sl. No	Applied Voltage V_{CC} (V)	I_B = 10µA		I_B = 20µA		I_B = 30µA	
		V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)	V_{CE} (V)	I_C (mA)
1							
2							
3							
4							
5							

Graph:



Input Characteristics



Output Characteristics

1. Plot the input characteristics for different values of $\mathbf{V_{CE}}$ by taking $\mathbf{V_{BE}}$ on X-axis and $\mathbf{I_B}$ on Y-axis taking $\mathbf{V_{CC}}$ as constant parameter.
2. Plot the output characteristics by taking $\mathbf{V_{CE}}$ on X-axis and taking $\mathbf{I_C}$ on Y-axis taking $\mathbf{I_B}$ as a constant parameter.

Procedure:

Input Characteristics:

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage V_{CE} as constant 2V by varying V_{CC}.
3. Varying V_{BB} gradually, note down base current I_B and emitter-base voltage (V_{BE}).
4. Step size is not fixed because of nonlinear curve. Initially vary V_{EE} in steps of 0.1 V. Once the current starts increasing vary V_{BB} in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for V_{CE} = 5V & 10V.

Output Characteristics:

1. Fix base current, I_B at constant value say 10µA.
2. Vary the output voltage V_{CC} in steps.
3. Measure the voltage V_{CE} and current I_C for different values.
4. Repeat above steps for I_B = 20µA, 30µA
5. Draw output static characteristics for tabulated values.

Result:

The h-parameters for a transistor in CB configuration are:

a. The Input resistance (h_{ib}) _____ Ohms.
b. The Reverse Voltage Transfer Ratio (h_{rb}) _____.
c. The Output Admittance (h_{ob}) _____ Mhos.
d. The Forward Current gain (h_{fb}) _____.

Conclusion:

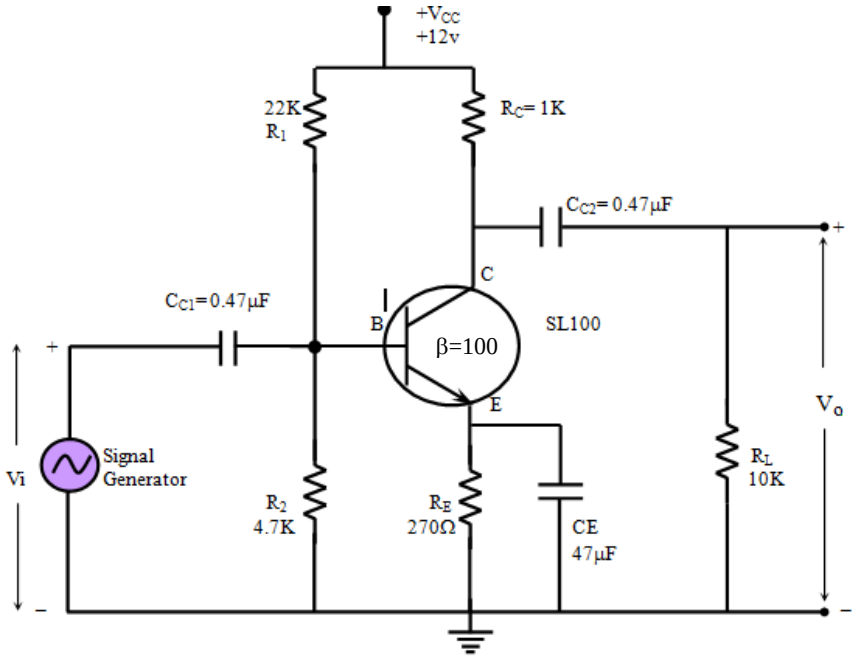
EXPERIMENT NO -3
SINGLE STAGE BJT RC – COUPLED AMPLIFIER

Aim: To find the Frequency response of single stage BJT and FET RC coupled amplifier and determination of half power points, bandwidth, input and output impedances.

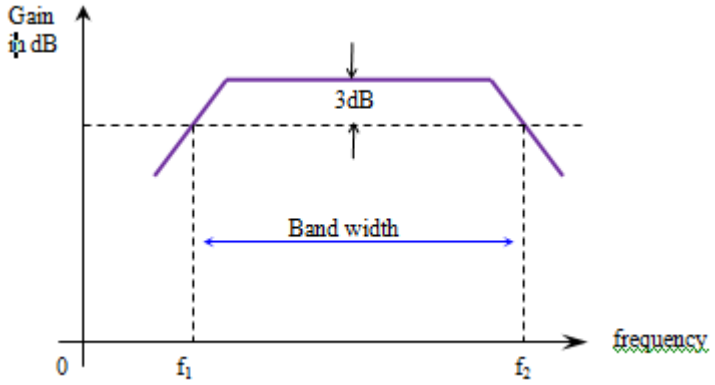
Apparatus Required:

S.N	Particulars	Type	Range	Quantity
1.	Transistor	SL100	-	01
2.	Capacitors	Electrolyte	0.47μF, 47μF	02 01
3.	Resistors	-	22KΩ,1KΩ,4.7KΩ 270Ω,10KΩ	01 Each
4.	Regulated Power Supply	DC	0-30V/2A	01
5.	Signal Generator	-	3MHz	01
6.	Oscilloscope and Probes	-	-	01
7.	Bread Board	-	-	01
8.	Connecting wires	Single Strand	-	few

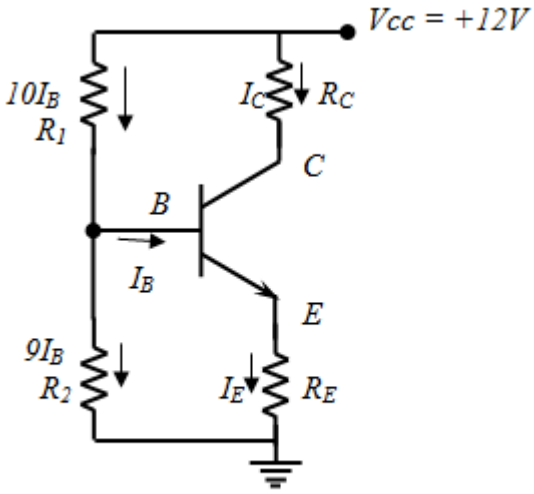
Circuit Diagram:



Frequency Response



Design:



Biasing Circuit

Let V_{CC} = 12V, I_C = 4.5mA, β= 100 (for SL100)

Calculation of R_E

$$V_{RE} = \frac{V_{cc}}{10} = \frac{12}{10} = 1.2V$$

That is $I_E R_E = 1.2V$

Therefore $$R_E = \frac{1.2}{I_E} = \frac{1.2}{I_c} = \frac{1.2}{4.5mA} = 0.267K\Omega$$

Use $R_E = 270\Omega$

Calculation of R_1 and R_2

From the biasing circuit

$V_B = V_{BE} + V_{RE} = 0.7 + 1.2 = 1.9Vs$

$I_B = \frac{I_C}{\beta} = \frac{4.5mA}{100} = 0.045mA$

Assume $10I_B$ flows through R_1 and $9I_B$ flows through R_2

$R_1 = \frac{V_{CC} - V_B}{10 I_B} = \frac{12 - 1.9}{10\ X\ 0.045} = 22.4K\Omega$

Use $R_1 = 22K\Omega$

Also we have

$V_B = V_{R2} = 9I_B \text{ x } R_2$

Therefore $R_2 = \frac{V_B}{9I_B} = \frac{1.9}{9x\ 0.045m} = 4.69K\Omega$

Use $R_2 = 4.7K\Omega$

Procedure:

1. Connect the biasing circuit as shown in the figure -2, set the RPS voltage Vcc = 12V. Measure the DC voltages (Using Oscilloscope) V_B at the base, V_C at the collector and V_E at the emitter with respect to ground. Then determine
   $V_{CE} = V_C - V_E =$ _____ V
   $I_C = \frac{V_{cc} - V_c}{R_c} =$ _____ mA (then Q point is given by V_{CE}, I_C)
2. Connect the RC coupled amplifier circuit shown in figure-1.
3. Apply the input sine wave at frequency say 10KHz from the signal generator and adjust peak –to-peak amplitude (Vi) of **20 to 50 milli volts** (till maximum undistorted sine wave output is obtained).
4. Vary the input sine wave frequency from 10Hz to 1MHz in suitable steps and measure the output voltage V_0 of the amplifier at each step using Oscilloscope(Keeping input amplitude remains constant throughout the frequency range) and record the readings in the tabular column.
5. Calculate the Gain in dB
6. Plot the graph of gain in dB v/s the frequency in semi log graph sheet and determine lower cutoff frequency (f_1) , upper cutoff frequency (f_2), mid band voltage gain Amid , and gain bandwidth product (GBW).

Procedure: For measuring the input impedance 'Z_i'

1. Connect the circuit as shown in fig.3
2. Set the following.
   i) DRB to its minimum value '0'
   ii) Input sine wave amplitude is kept at 50mV.
   iii) Frequency around 10 kHz.
   iv) Measure p-p V_o
3. Let $V_o = V_a$, Increase DRB till $V_o = V_a/2$. So that the corresponding DRB value gives the input impedance 'Z_i' of the RC Coupled amplifier.

Calculation of R_C

Choose $V_{CE} = \frac{V_{cc}}{2} = \frac{12}{2} = 6V$

From the biasing circuit

$$V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$$

$$12 - 4.5R_C - 6 - 1.2 = 0$$

Therefore $R_C = 1.07K\Omega$

Use $R_C = 1\ K\Omega$

Calculation of Bypass capacitor (C_E) and coupling capacitors (C_{C1} and C_{C2})

Let $X_{CE} = \frac{1}{10} R_E$ at frequency f =100Hz

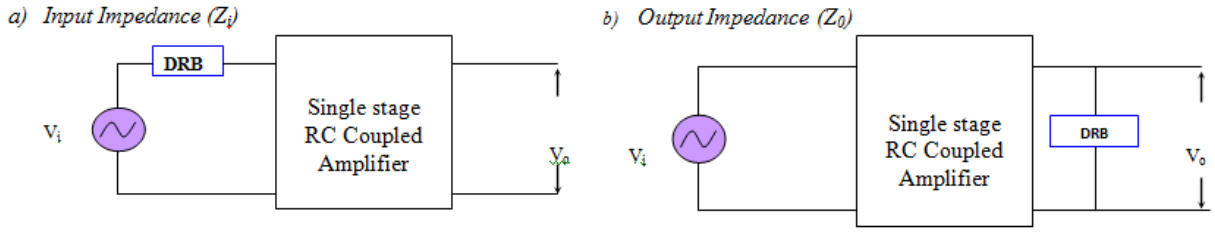
That is $\frac{1}{2\pi f X\ C_E} = \frac{R_E}{10}$

Therefore $C_E = \frac{10}{2\pi f X\ R_E} = \frac{10}{2\pi\ X\ 100\ X\ 270} = 59\mu F$

Use standard value $C_E = 47\mu F$ (Electrolytic)

Also use C_{C1} and $C_{C2} = 0.1\mu F$ (ceramic)

ii) Determination of Input Impedance (Z_i) and Output Impedance (Z_0)



Procedure: For measuring the output impedance 'Z_O'

1. Connect the circuit as shown in fig.4
2. Set the following.
   i. DRB to its Maximum value.
   ii. Input sine wave amplitude is kept at 50mV
   iii. Frequency around 10 kHz.
   iv. Measure p-p V_o
   Let $V_o = V_b$, Decrease DRB till $V_o = V_b/2$
3. So that the corresponding DRB value gives the Output impedance 'Z_o' of the RC Coupled amplifier

Results:

- Mid band voltage gain = _____
- Mid band voltage gain in dB = _____dB
- Lower cutoff frequency = _____HZ
- Upper cutoff frequency = _____Hz
- Band width = _____Hz
- Gain Bandwidth Product = _____Hz
- Input Impedance = _____Ω
- Output Impedance = _____Ω

Conclusion:

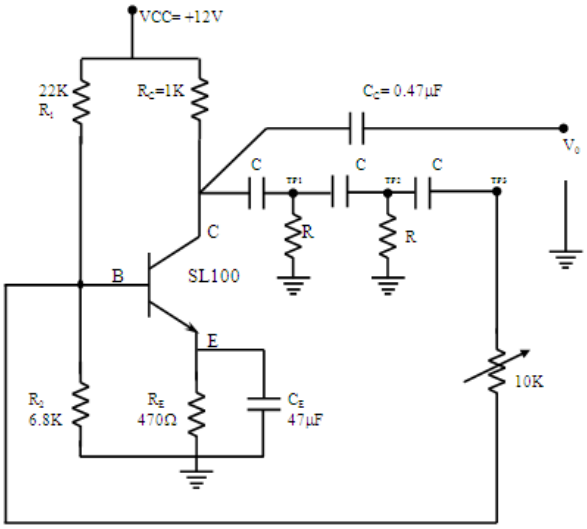
EXPERIMENT NO 4
RC PHASE SHIFT OSCILLATOR

Aim: To design and verify the performance of RC Phase shift Oscillator.

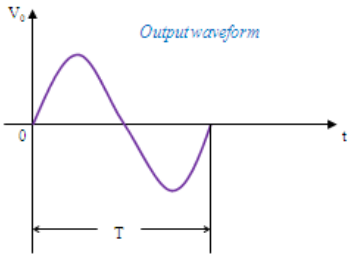
Apparatus required:

S.N	Particulars	Type	Range	Quantity
1.	Transistor	SL100	-	01
2.	Capacitors	Ceramic Electrolytic	0.01μF 47μF, 0.47μF	03 01
3.	Resistors	-	22KΩ 6.8KΩ 1KΩ 2.2KΩ 470 Ω	01 01 01 02 01
4.	Regulated Power Supply	DC	0-30V/2A	01
5.	Potentiometer	-	10 KΩ	01
6.	Oscilloscope and Probes	-	-	01
7	Bread Board	-	-	01
8	Connecting wires	-	-	few

Circuit diagram:



SPECIMEN GRAPH:



Design:

Amplifier design:

Let V_{CC} *= 12V,* I_C *= 4mA,* h_{fe} *= 100 (for SL100)*

Let V_E *= 2V,* V_{CE} *= 6V*

Therefore $R_E = \frac{V_E}{I_E} = \frac{V_E}{I_C} = \frac{2}{4mA} = 0.5K\Omega = 500\Omega$

Use $\boldsymbol{R_E = 470\Omega}$

R_C: From the biasing circuit (apply KVL to CE loop)

V_{CC}- I_CR_C-V_{CE}-V_E = 0

12- 4R_C-6-2 =0

Therefore $\boldsymbol{R_C = 1\ K\Omega}$

Calculation of R_1 AND R_2

From the biasing circuit

$$V_B = V_{CC} x \frac{R_2}{R_1+R_2}$$

We know that $V_B = V_{BE} + V_E$

$V_B = 2 + 0.7 = 2.7V$

Therefore $\frac{V_B}{V_{CC}} = \frac{R_2}{R_1+R_2}$

$\frac{2.7}{12} = \frac{R_2}{R_1+R_2}$

$0.225 = \frac{R_2}{R_1+R_2}$

$0.225R_1 + 0.225R_2 = R_2$

$R_1 = 3.44R_2$

If $\boldsymbol{R_2 = 6.8\ K\Omega}$, *then* $R_1 = 23.3K\Omega$, *Use* $R_1 = 22K\Omega$

Use $\boldsymbol{C_E = 50\mu F \text{ or } 47\ \mu F}$ *(Electrolytic)*

Also use $\boldsymbol{C_C = 0.1\mu F}$ *(ceramic)*

Design of shifting network

The frequency of oscillations is determined by phase shifting network. The oscillating frequency for the above circuit is given by

$$f_0 = \frac{1}{2\pi RC\sqrt{6+4K}}$$

Where $K = \frac{R_C}{R}$ *which is usually < 1*

Let $\boldsymbol{f_0 = 2\ KHz}$ *(Audio frequency range 20Hz to 20KHz) and* $\boldsymbol{R = 2.2\ K\Omega}$

Therefore $K = \frac{R_C}{R} = \frac{1K}{2.2K} = 0.454$

Therefore $f_0 = \frac{1}{2\pi RC\sqrt{6+4(0.454)}}$

$C = 0.0121\ \mu F$; $\boldsymbol{Use\ C = 0.01\ \mu F}$

Note:

The last resistor in the phase shifting network is chosen to be a 10K pot. This is to get an overall phase shift of 180^o at frequency of oscillations.

The minimum h_{fe} required for the transistor to oscillate is

$$h_{fe(min)} = 23 + 29\,x\,\frac{R}{R_C} + 4\,x\,\frac{R_C}{R}$$

Where $R_C = 1K\Omega$ and $R = 2.2K\Omega$ (Phase shifting network)

Therefore $$h_{fe(min)} = 23 + 29\,x\,\frac{2.2K}{1K} + 4\,x\,\frac{1K}{2.2K}$$

$$h_{fe(min)} = 89$$

Procedure:

1. Connections are made as per the circuit diagram.
2. Switch ON the power supply and set the biasing voltage V_{CC} =12V.
3. Adjust the 10KΩ pot to get a stable sinusoidal output and observe the sine wave form on oscilloscope.
4. Measure the frequency of oscillations of the output from the oscilloscope, then compare with theoretical value.
5. With respect to the output Vo, the waveforms at points TP_1, TP_2 and TP_3, are observed on oscilloscope. We can see the phase shift at each point being shifted by an angle 60^0, 120^0, 180^0.
6. Draw the waveform on graph sheet.

Result:

Theoretical frequency of oscillations = _____KHz

Practical frequency of oscillations = _____KH

Conclusion:

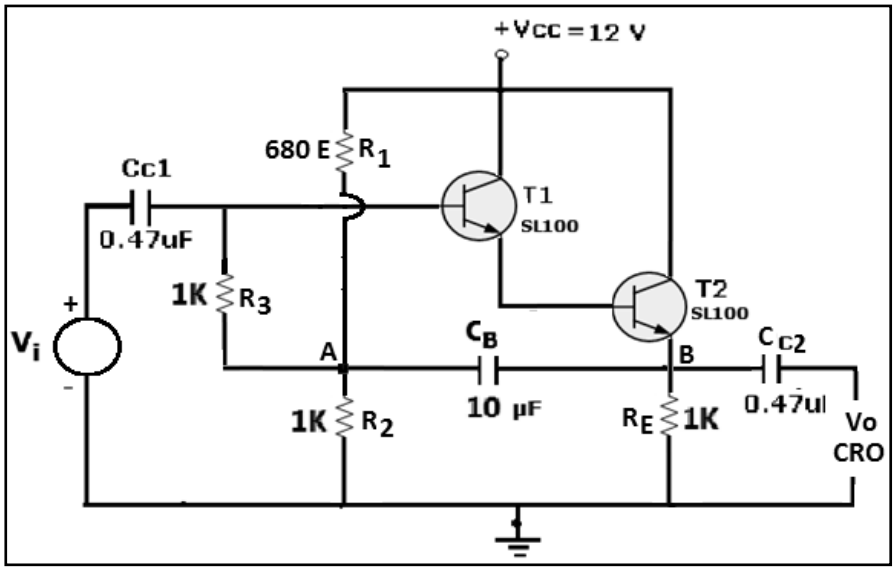
EXPERIMENT NO -5
BJT DARLINGTON EMMITTER FOLLOWER

AIM: To determination of gain, input and output impedance of BJT Darlington emitter follower with and without bootstrapping.

APPARATUS REQUIRED:

S.N	Particulars	Type	Range	Quantity
1.	Transistor	SL100	-	02
2.	Capacitors	Ceramic Electrolytic	10 μF 47μF	01 02
3.	Resistors	-	1 KΩ 680 Ω	03 01
4.	Regulated Power Supply	DC	0-30V/2A	01
5.	Signal Generator	-	3 MHz	01
6.	Voltmeter	-	0-30 V	02
8.	CRO and Probes	-	-	01
9.	Bread Board	-	-	01
10.	Connecting wires	-	-	few

CIRCUIT DIAGRAM:



Design:

Let V_{CC} = 12 V D.C.; $I_{C2} \approx I_{E2}$ = 6mA, $h_{fe}1$ = 50, $h_{fe}2$ = 100;

Choose VCE2 = VCC / 2 = 12/2 = 6V;

$I_{B2}=I_{C2}/h_{fe}2$ = 6000/100 = 60μA = I_{C1};

$I_{B1} = I_{C1}/h_{fe1}$= 60/50 = 1.2μA

$R_E = (V_{CC} - V_{CE2})/I_{E2}$ =6V / 6mA = 1000 Ω

Assume R_3 = 1K, then R_3I_{B1} = 1.2 mV.

$V_{AG} = V_{AB1} + V_{BE1} + V_{BE2} + V_{E2}$
$= R_3I_{B1} + V_{BE1} + V_{BE2} + V_{E2}$
=1.2 mV + 0.7 V + 0.7 V + 6V
=7.4012 V

With R_2 = 1 K, $I_{R2} = V_{AG}/R_2$ = 7.4012 mA=7401.2 μA, let R_2 = 1 K
Therefore, $I_{R1} = I_{R2} + I_{B1}$ =7401.2 + 1.2 = 7402.4 μA
$R_1= (V_{CC}-V_{AG})/I_{R1}$ = 12-7.4012/7402.4 μA =621.258Ω; let R1 = 680 Ω
Choose $C_{C1} = C_{C2}$ = 0.47 μF.

PROCEDURE:
To measure Voltage Gain
1. Connect the circuit as shown in the figure
2. Switch on the power supply and set V_{CC} = +12 V.
3. Measure the DC Voltages using CRO or Multimeter and record.

	VCE1	VBE1	VCE2	VBE2	VE2
Assumed	6V	0.7V	6V	0.7V	6V
Obtained					

4. Apply a sine wave voltage from the Function Generator.
5. Observe the o/p Vo. Measure and record Vi and Vo. Compute and enter the voltage gain, $A_V=V_O/V_I$ in the table.

Voltage gain with bootstrap

Vi							**Vi, max**
Vo							
Av							

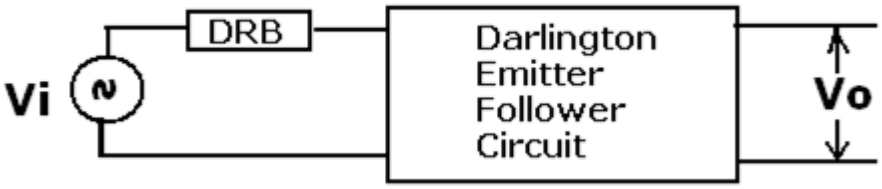
Record V_i, Max, The maximum input you can apply for undistorted output as the "Maximum Signal handling capacity" of the Emitter follower.
6. Repeat the experiment after disconnecting the capacitor CB in branch AB, i.e.; just remove the Bootstrapping capacitor, CB. Now you have taken away the Bootstrapping.

Voltage gain without bootstrap

Vi							**Vi, max**
Vo							
Av							

To measure Input Impedance Z_i:

1. Connect the circuit as shown below.



2. Set the DRB to minimum (0 Ω). Apply a10 KHz sine wave signal of amplitude 1V (p-p) or any suitable value to get an undistorted output.
3. Measure V_O (p-p). Let V_O = Va (say) with DRB value = 0
4. Increase DRB value in steps till $V_O = V_A/2$. The corresponding DRB value gives Z_I.
5. Repeat the experiment by disconnecting CB, the bootstrapping capacitor.
6. Compare the two input impedance values you have measured.

To measure output impedance, Zo:

1. Connect the circuit as shown in figure

2. Set the DRB to its maximum resistance value. Apply a 10 KHz sine wave of amplitude1V (p-p) or any suitable value to get undistorted output
3. Measure V_O (p-p), $V_O = V_B$ without DRB connection or DRB value at Max.
4. Decrease DRB value in steps till $V_O = V_B/2$. The corresponding DRB value gives Z_O.
5. **In this part of the experiment, it is likely that the o/p wave form may get distorted as the DRB value is decreased. Then, V_I has to be set to a lower value and the steps**

to be repeated. Note carefully that the answer will be wrong if you take readings with distorted output.

6. Repeat the experiment by disconnecting the Bootstrapping capacitor.

RESULT:

1. Voltage Gain with Boot Strap. : …….
2. Voltage Gain with Boot Strap. : …….
3. Input Impedance, Zi, with Bootstrap. : …….
4. Input Impedance, Zi, without Bootstrap. : …….
5. Output Impedance, Z0, with Bootstrap. : ……
6. Output Impedance, Z0, without Bootstrap. : …….
7. Current Gain, Ai, With Bootstrap. : ……
8. Current Gain, Ai, Without Bootstrap. : …….

$$V_i = Z_i \times I_i,\ V_o = Z_o \times I_o \square\ A_i = (I_o/I_i) = A_V \times (Z_i/Z_o)$$

CONCLUSION:

EXPERIMENT NO 6
Simplification & Realization of Boolean Expressions

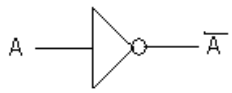
Aim: Simplification, realization of Boolean expressions using logic gates/Universal gates.

Components Required:

Sl. No	Name of the Component	IC number	Qty
1	AND gate	7408	2
2	OR gate	7432	2
3	Not gate	7404	2
4	EXOR gate	7486	2
5	NAND gate	7400	2
6	NOR gate	7402	2
7	EX-NOR gate	4077	1
8	Patch chords		few
9	Trainer Kit		

NOT GATE

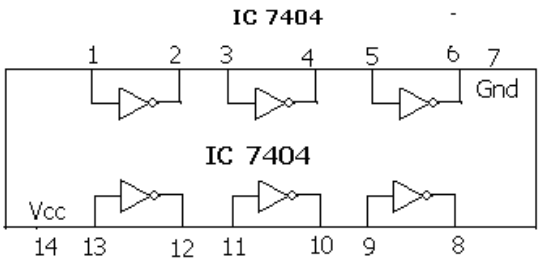
SYMBOL



TRUTH TABLE

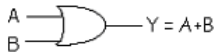
Dec	I/P (A)	O/P $\overline{(A)}$
0	0	1
1	1	0

IC 7404



OR GATE

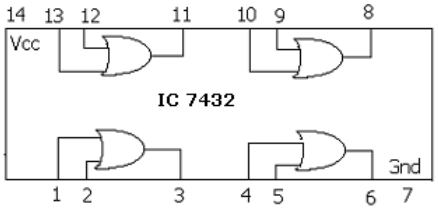
SYMBOL



TRUTH TABLE

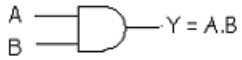
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

IC 7432



AND GATE

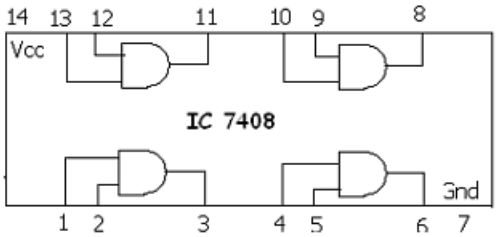
SYMBOL



TRUTH TABLE

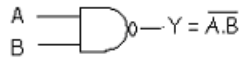
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	1

IC 7408



NAND GATE

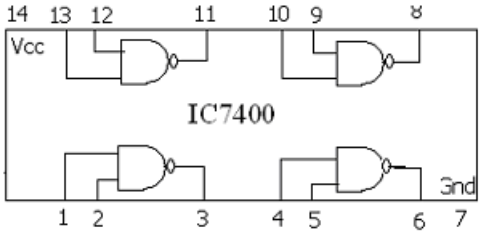
SYMBOL



TRUTH TABLE

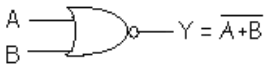
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	1
2	1	0	1
3	1	1	0

IC 7400



NOR GATE

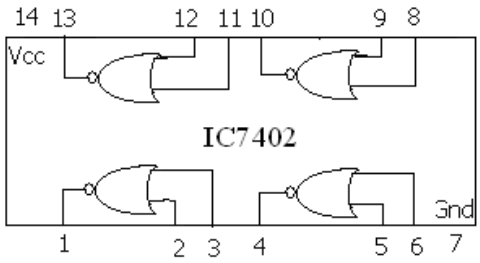
SYMBOL



TRUTH TABLE

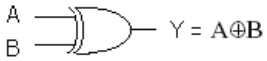
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	0

IC7402



XOR GATE

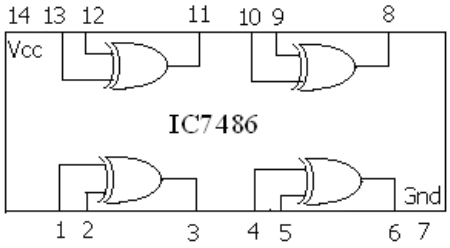
SYMBOL



TRUTH TABLE

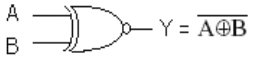
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

IC- 7486



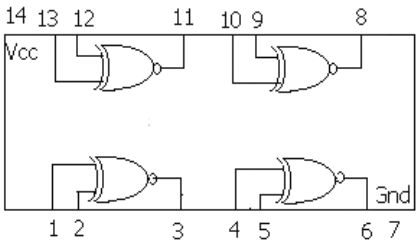
EX-NOR GATE

SYMBOL



TRUTH TABLE

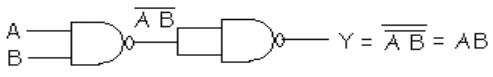
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	1



Implementation of Basic Gates Using Universal Gates

NAND gate as **AND** gate

Logic Diagram

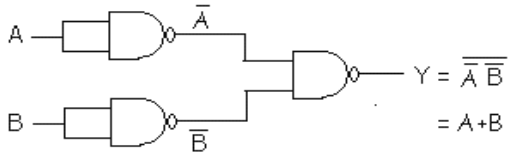


Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	1

NAND gate as **OR** gate

Logic Diagram



Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

NAND gate as **NOT** gate

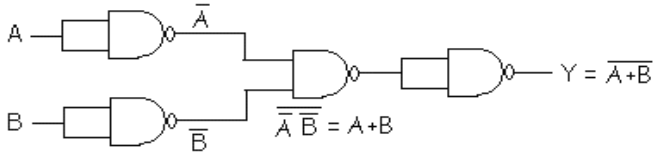
Logic Diagram

Truth Table

Dec Eq	I/P (A)	O/P $\overline{(A)}$
0	0	1
1	1	0

NAND gate as **NOR** gate

Logic Diagram

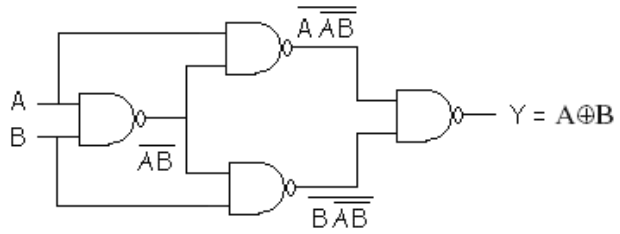


Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	0

NAND gate as **Ex-OR** gate

Logic Diagram



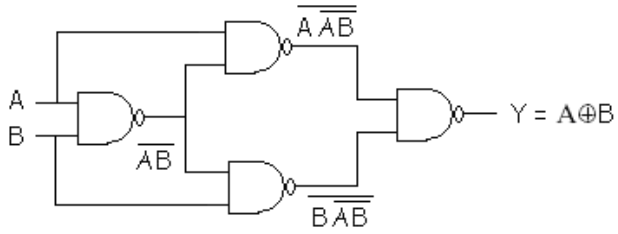
Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

$\overline{A\,\overline{AB}}\;\overline{B\,\overline{AB}} = [\overline{A}+\overline{B}]\;\overline{AB} = [A+B][\overline{A}+\overline{B}] = [A\overline{B}+\overline{A}B] = A\oplus B$

NAND gate as **Ex-NOR** gate

Logic Diagram



Truth Table

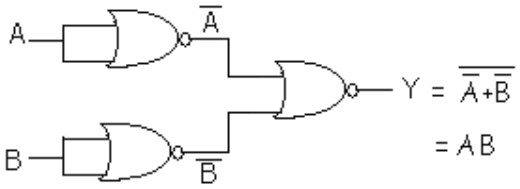
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

$\overline{A\,\overline{AB}}\;\overline{B\,\overline{AB}} = [\overline{A}+\overline{B}]\;\overline{AB} = [A+B][\overline{A}+\overline{B}]$

$= [A\overline{B}+\overline{A}B] \quad = A\oplus B$

NOR gate as **AND** gate

Logic Diagram

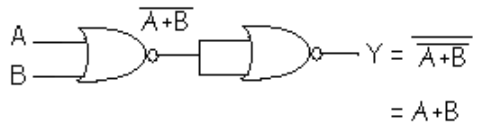


Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	1

NOR gate as **OR** gate

Logic Diagram

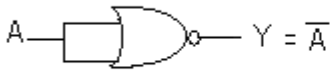


Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

NOR gate as **NOT** gate

Logic Diagram

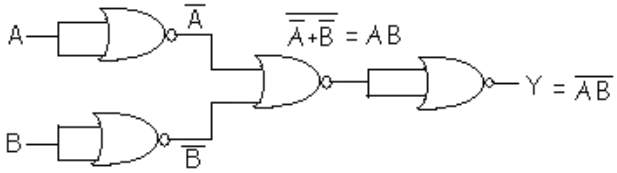


Truth Table

Dec Eq	I/P (A)	O/P $\overline{(A)}$
0	0	1
1	1	0

NOR gate as **NAND** gate

Logic Diagram

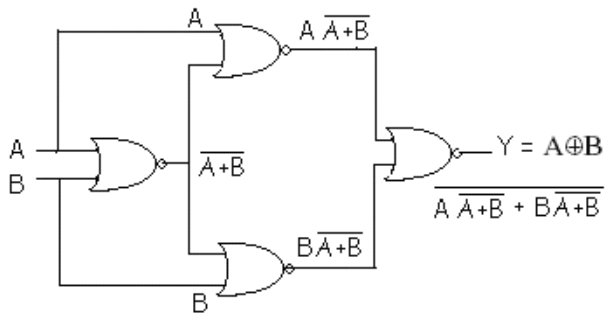


Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	1
2	1	0	1
3	1	1	0

NOR gate as **Ex-NOR** gate

Logic Diagram

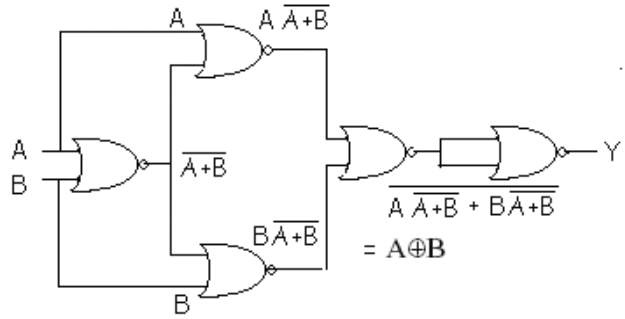


Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

NOR gate as **Ex-OR** gate

Logic Diagram



Truth Table

Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	1

Realize the following expressions in

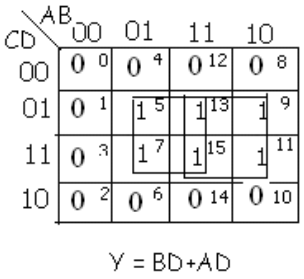
(1) SOP form (sum of product)

(2) POS form (product of sum)

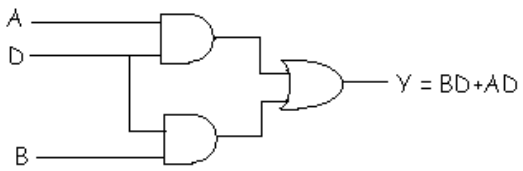
SOP FORM

F(A,B,C,D) = ∑(5,7,9,11,13,15)

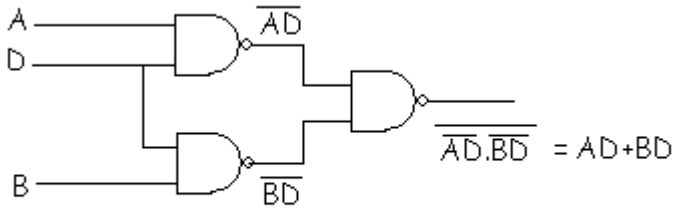
Simplification- SOP form



using basic gates



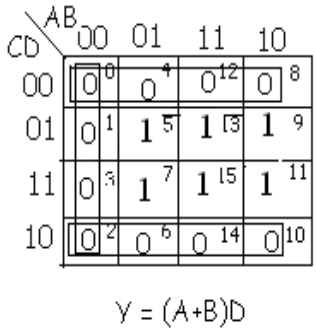
Using NAND gates



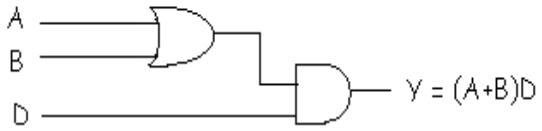
POS FORM

$F(A,B,C,D) = \prod(0,1,2,3,4,6,8,10,12,14)$

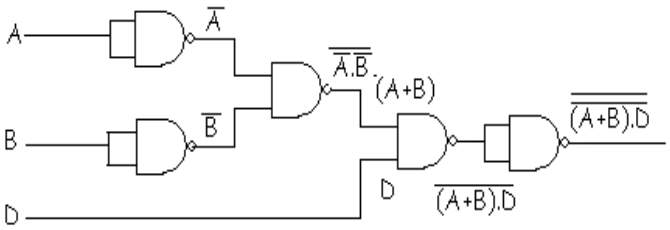
Simplification- POS form



Using basic gates



Using NAND gates



Procedure:

1. Place the IC in the socket of the trainer kit.
2. Complex Boolean Expressions are simplified by using K maps.
3. Make the connections as shown in the circuit diagram.
4. Apply different combinations of inputs according to the truth table and verify the outputs.
5. Repeat the above procedure for all the circuit diagrams.

Truth table:

Dec Eq	INPUTS				O/P
	A	B	C	D	Y=(A+B) D
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1

CONCLUSION:

EXPERIMENT NO 7
Half/ Full Adder & Subtractor

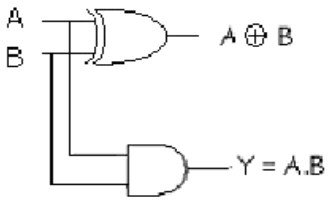
Aim: Realization of half/Full adder and Half/Full Subtractors using logic gates.

Components Required:

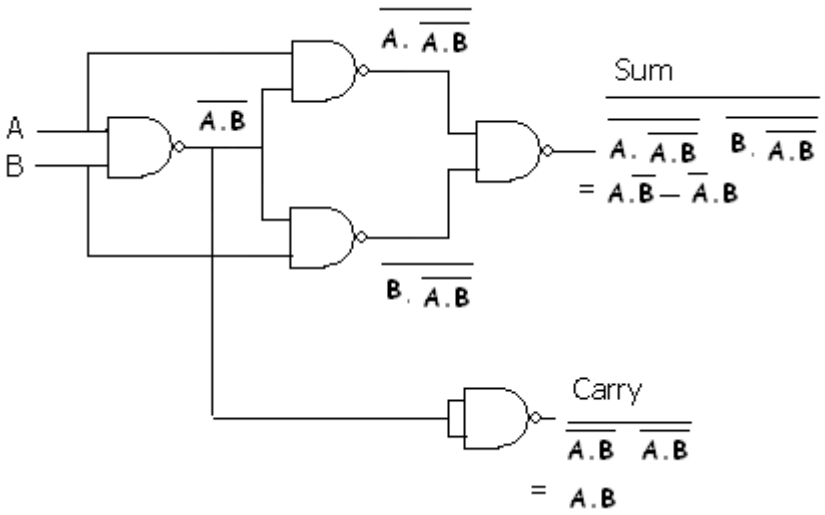
Sl. No	Name of the Component	IC number	Qty
1	AND gate	7408	1
2	OR gate	7432	1
3	Not gate	7404	1
4	EXOR gate	7486	3
5	NAND gate	7400	3
6	NOR gate	7402	3
7	Patch chords		Few
8	Trainer Kit		

Half Adder Using Basic Gates

Truth Table				
DEC EQ	INPUTS		OUTPUTS	
	A	B	SUM	CARRY
0	0	0	0	0
1	0	1	1	0
2	1	0	1	0
3	1	1	0	1



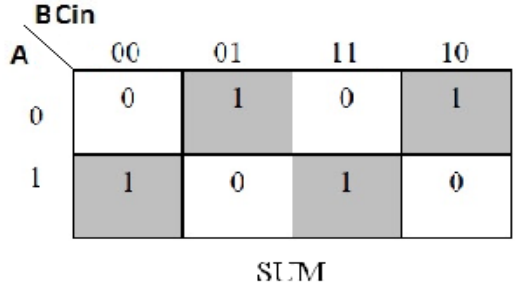
Half Adder Using NAND Gates

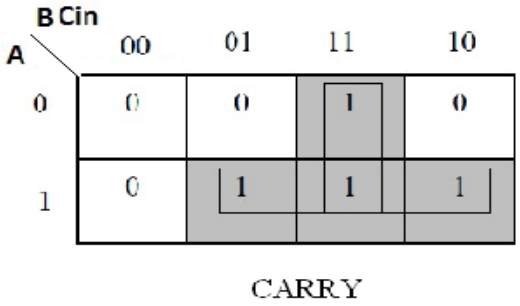


Full Adder:

Truth Table

Dec Eq	Inputs			Outputs	
	A	B	Cin	Sum	Carry
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1





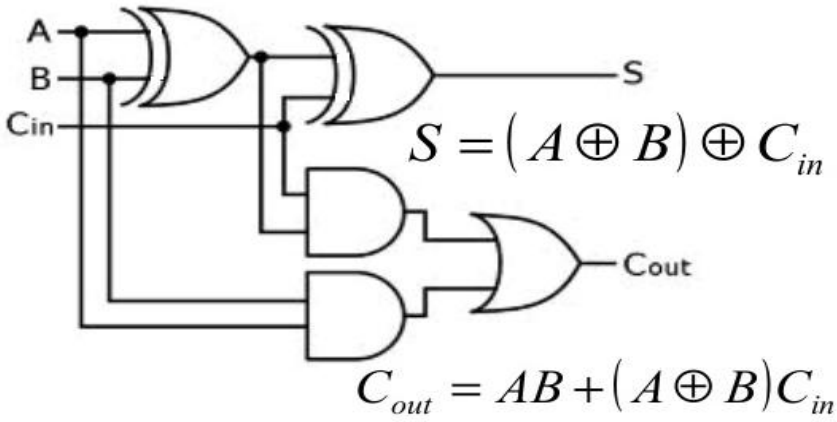
$$SUM = \bar{A}\bar{B}Cin + AB\bar{C}in + A\bar{B}\bar{C}in$$

$$SUM = Cin\,(\bar{A}\bar{B} + AB) + \bar{C}in\,(\bar{A}B + A\bar{B})$$

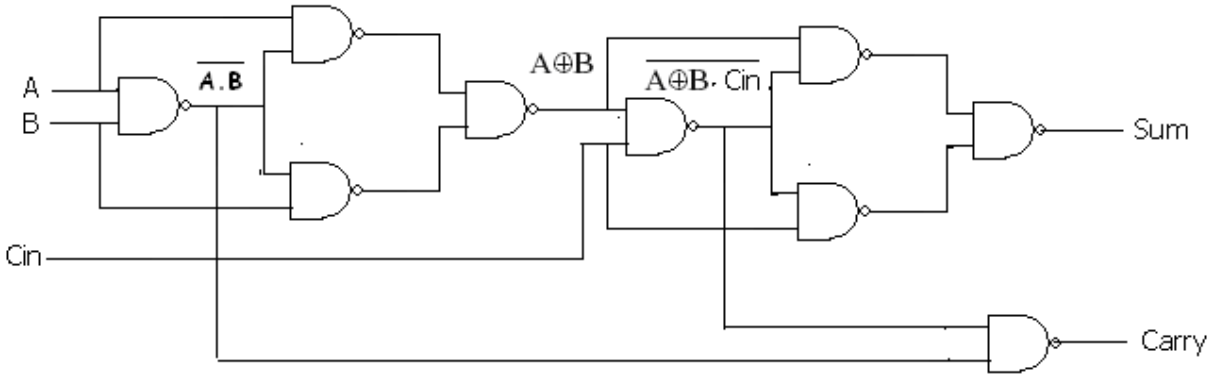
$$SUM = Cin\ XOR\ (A\ XOR\ B)$$

or $Cout = Cin\,(A\ XOR\ B) + AB$

Logic Diagram Using Basic Gates



Using NAND Gates:

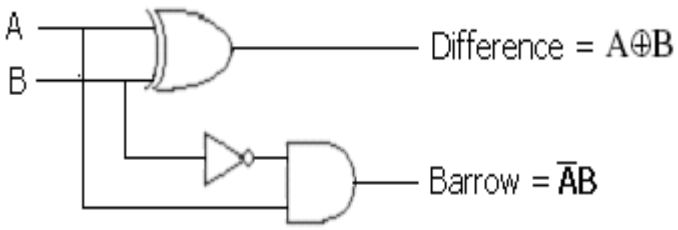


Half Subtractor

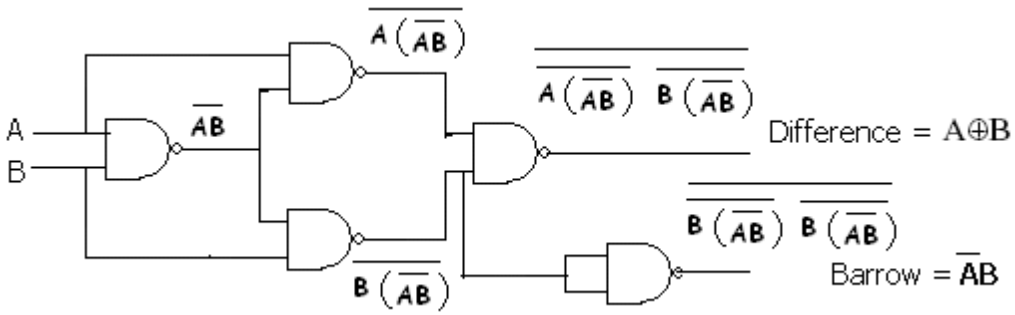
Truth Table

Dec Eq	INPUTS		OUTPUTS	
	A	B	Diff	Barrow
0	0	0	0	0
1	0	1	1	1
2	1	0	1	0
3	1	1	0	0

Circuit Diagram



Using NAND gates



Full Subtractor

Truth Table

Dec Equi	Inputs			Outputs	
	A	B	Bin	Diff	Borrow
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

$Diff = \bar{A}\,\bar{B}\,Bin + \bar{A}\,B\,\overline{Bin} + A\,\bar{B}\,\overline{Bin} + A\,B\,Bin$

$= (\bar{A}\,\bar{B} + A\,B)Bin + (\bar{A}\,B + A\,\bar{B})\,\overline{Bin}$

$= (A \odot B)\,Bin + (A \oplus B)\overline{Bin}$

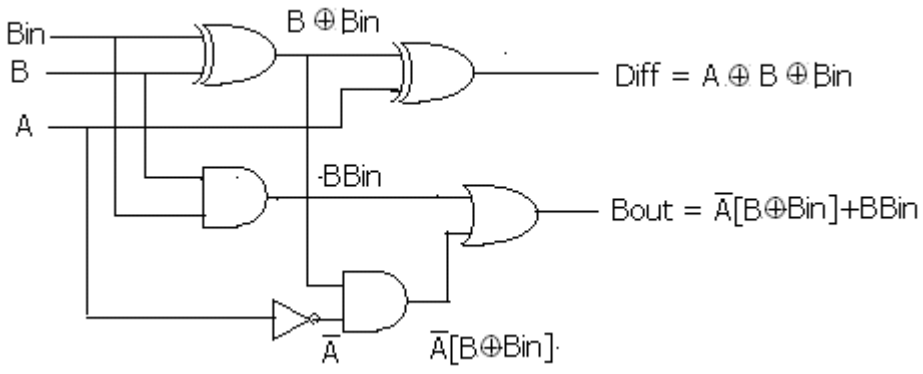
$Diff = A \oplus B \oplus Bin$

$Bout = \bar{A}\,\bar{B}\,Bin + \bar{A}\,B\,\overline{Bin} + \bar{A}\,B\,Bin + A\,B\,Bin$

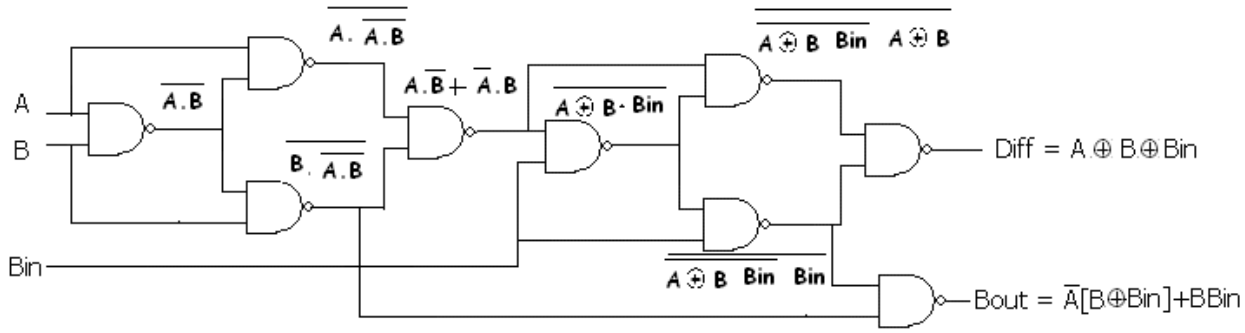
$= \bar{A}\,[\bar{B}\,Bin + B\overline{Bin}] + [A + \bar{A}]\,B\,Bin$

$Bout = \bar{A}\,(B \oplus Bin) + B\,Bin$

Logic Diagram



Using NAND Gates



Procedure:

1. Obtain the Boolean Expressions for Half/Full adder and subtractor (sum & Carry) by writing the truth table and simplifying with the help of K-map.
2. Make the connections as shown in the logic diagram.
3. Apply different combinations of inputs according to the truth table and verify the outputs.
4. Repeat the above procedure for all the circuit diagrams.

Conclusion:

EXPERIMENT NO 8
Parallel Adder/Subtractor and Code Conversion

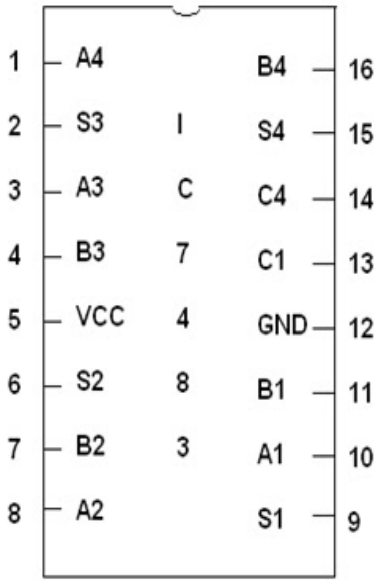
AIM: (1) Realization of Parallel adder/subtractor using 7483chip

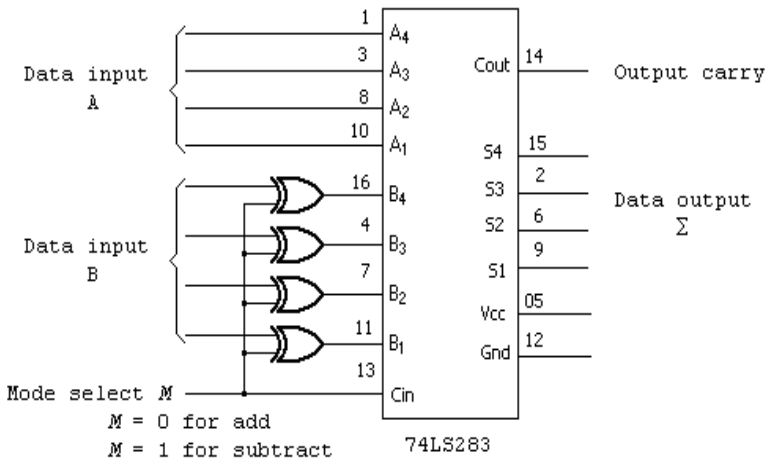
(2) BCD to EXCESS-3 code conversion and vice versa

Aim: Realization of Parallel adder/subtractor using 7483chip
Components required:

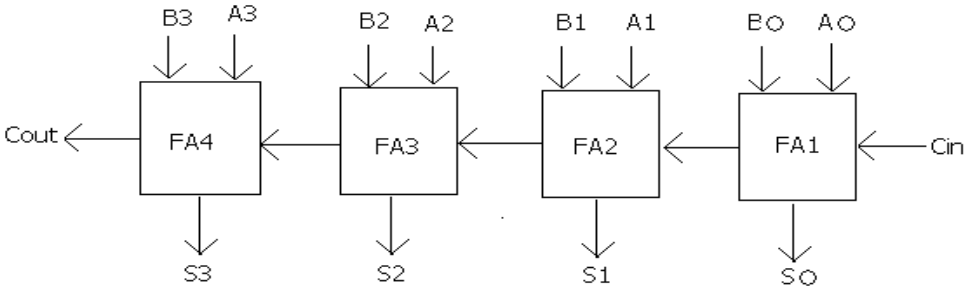
Sl. No	Component	IC number	Qty
1	EXOR gate	7486	1
2	4 bit parallel adder/subtractor	7483	1
3	Patch chords		few
4	Trainer Kit		

Pin diagram & Logic diagram





Block Diagram



Procedure:

1. Make the connections as per logic diagram.
2. For addition, make C_{in}=0 and apply the 4 bits as input A and apply another set of 4-bits as B. Observe the output at S_3, S_2 S_1 S_0 and carry generated at C_{out}.
3. Repeat the above steps for different inputs and tabulate the result.
4. For subtraction C_{in} is made 1.
5. Verify the difference. S_3, S_2 S_1 S_0 and C_{out}.
   If C_{out} is 0, diff is negative and diff is 2's complement form.
   If C_{out} is 1, diff is positive.
6. Repeat the above steps for different inputs and tabulate the result.

Readings:

C_{in}	Inputs								Outputs				
	A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	Carry C_{out}	S_4	S_3	S_2	S_1
0 for addition	1	0	0	1	1	0	0	1	1	0	0	1	0
	0	1	1	1	0	0	0	1	0	1	0	0	0
1 for subtraction	1	0	0	1	1	0	0	0	1	0	0	0	1
	0	0	0	1	0	0	1	1	0	1	1	1	0

Conclusion:

Aim: Realization of BCD to Excess-3 code conversion and vice versa.

Truth table

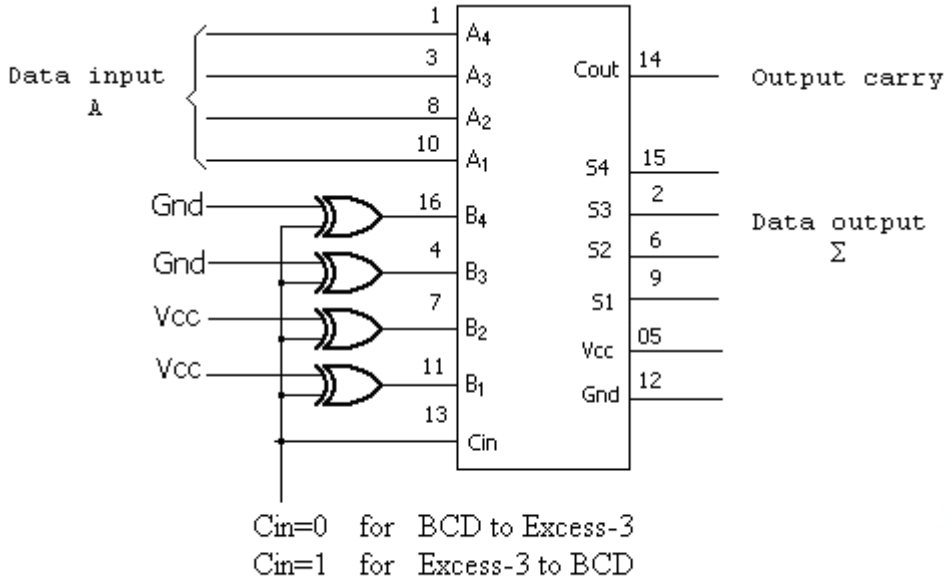
BCD to Excess-3

BCD (Inputs)				Excess-3 (Outputs)			
A4	A3	A2	A1	X4	X3	X2	X1
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Excess-3 to BCD

Excess-3 (Inputs)				BCD (Outputs)			
X4	X3	X2	X1	S4	S3	S2	S1
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

Circuit Diagram



Procedure:

1. Write Truth table for BCD to Excess-3 as well as Excess-3 to BCD conversion.
2. Obtain the simplified boolean expression using k-map.
3. Connections are made as per the logic diagram
    - For BCD to Excess –3 code conversion →3 has to be added to input bits. make Cin =0.
    - For Excess-3 to BCD code conversion→3 has to be subtracted from the input therefor Cin =1.
4. Apply different combinations of inputs and verify the truth table.

Conclusion

EXPERIMENT NO 9

Binary to Gray and Gray to Binary code conversion

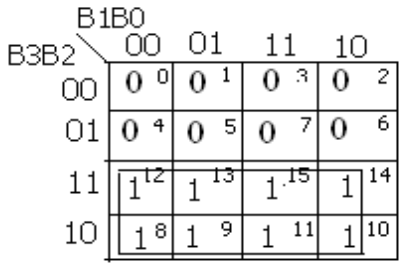
Aim: Realization of Binary to Gray code conversion and vice versa.

Components Required:

Sl.No	Name of the component	IC Number	Quantity
1	EXOR gate	7486	1
2	NAND gate	7400	4
3	Patch chords		Few
4	Trainer Kit		

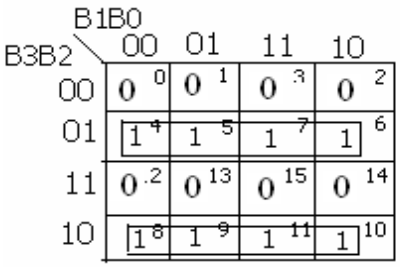
Binary to Gray code

G3 = ∑(8,9,10,11,12,13,14,15)



G3=B3

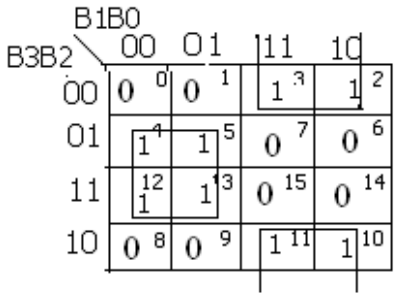
G2 = ∑(4,5,6,7,8,9,10,11)



$\overline{B3}B2 + B3\overline{B2}$

$B3 \oplus B2$

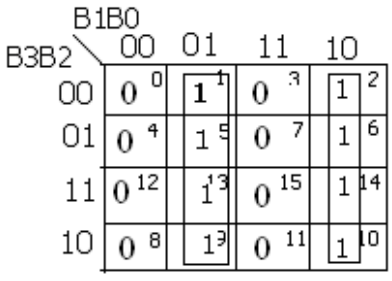
G1= ∑(2,3,4,5,10.,11,12,13)



$G1 = B2\overline{B1} + \overline{B2}B1$

$G1 = B1 \oplus B2$

G0 = ∑(1,2,3,5,6,9,10,13,14)



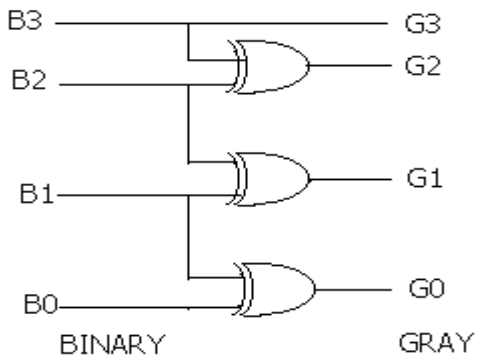
$G0 = \overline{B1}B0 + B1\overline{B0}$

$G0 = B1 \oplus B0$

Truth Table:

BINARY				GRAY CODE			
Inputs				Outputs			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Using XOR Gates:

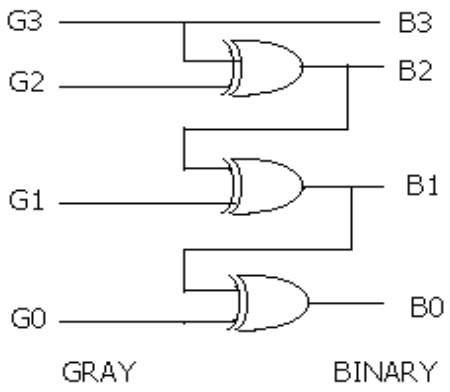


GRAY TO BINARY

Truth Table:

GRAY CODE				BINARY CODE			
Inputs				Outputs			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

Logic Diagram:



Procedure:

1. Write Truth table for Binary to Gray code as well as Gray code to Binary conversion.
2. Obtain the simplified boolean expression using k-map.
3. Connections are made as per the logic diagram
4. Apply different combinations of inputs and verify the truth table.

Conclusion

EXPERIMENT NO 10
Ring & Johnson Counters

Aim: Design and testing of Ring counter/Johnson counter using IC-7495

RING COUNTER USING IC-7495

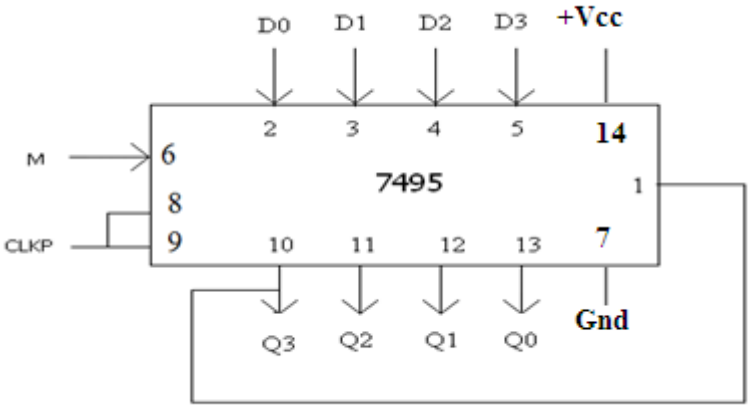
Components Required:

Sl.No	Name of the Component	IC number	Quantity
1	Ring Counter	7495	1
2	NOT gate	7404	1
3	Patch chords		few
4	Trainer Kit		

Truth Table

Input	Outputs			
Clock Pulse	Q0	Q1	Q2	Q3
t0	1	0	0	0
t1	0	1	0	0
t2	0	0	1	0
t3	0	0	0	1
t4	1	0	0	0

Circuit Diagram



Procedure:

1. Connections are made as shown in the logic diagram.
2. The data 1 0 0 0 is applied at D0, D1, D2 & D3 respectively.
3. Keeping the mode M=1, one clock pulse is applied. The data 1 0 0 0 appears at Q0, Q1, Q2 & Q3.
4. Keeping M=0, clock pulses are applied and truth table is verified.

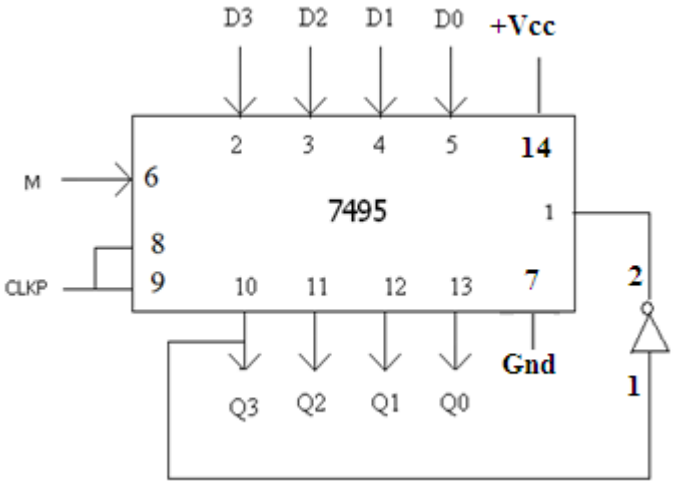
.

JHONSON COUNTER USING IC-7495

Truth Table

Input	Outputs			
Clock Pulse	Q0	Q1	Q2	Q3
t0	1	0	0	0
t1	1	1	0	0
t2	1	1	1	0
t3	1	1	1	1
t4	0	1	1	1
t5	0	0	1	1
t6	0	0	1	1
t7	0	0	0	1
t8	1	0	0	0

Circuit Diagram



Procedure:

1. Connections are made as shown in the logic diagram.
2. The data 1 0 0 0 is applied at D3, D2, D1 & D0 respectively.
3. Keeping the mode M=1, one clock pulse is applied. The data 1 0 0 0 appears at Q0, Q1, Q2 & Q3 respectively.
4. Keeping M=0, clock pulses are applied and truth table is verified.

Conclusion:

EXPERIMENT NO 11
Sequence Generator

Aim: Design and testing of Sequence generator.
Take the sequence as: **100010011010111**

Design: There are 15 bits, so there will be 15 states s=15. So at least 4 flip-flops are required.

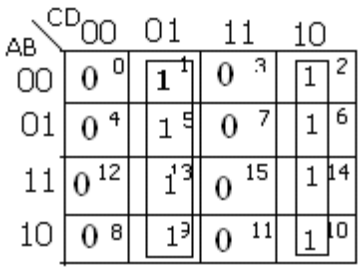
Components Required:

Sl. No	Name of the Component	IC Number	Quantity
1	Shift register	7495	1
2	Ex-OR	7486	1
3	Trainer Kit		1
4	Patch Chords		few

Truth Table

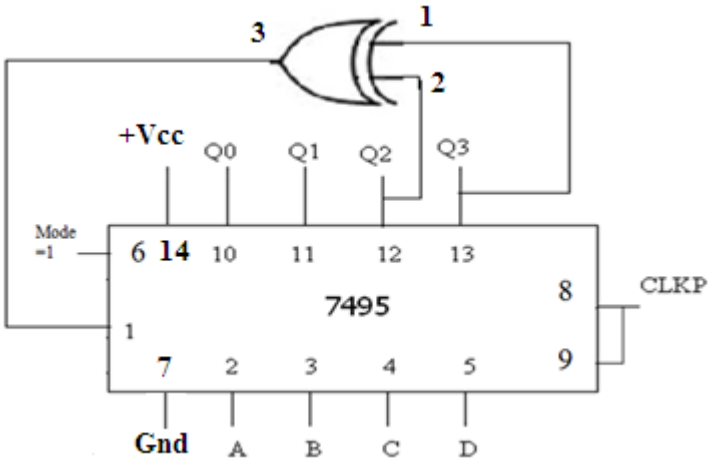
Sl. No.	**Outputs**			
	A	**B**	**C**	**D**
1	1	1	1	1
2	0	1	1	1
3	0	0	1	1
4	0	0	0	1
5	1	0	0	0
6	0	1	0	0
7	0	0	1	0
8	1	0	0	1
9	1	1	0	0
10	0	1	1	0
11	1	0	1	1
12	0	1	0	1
13	1	0	1	0
14	1	1	0	1
15	1	1	1	0

Simplification



$F = \overline{C}D + C\overline{D}$

$F = C \oplus D$



Procedure:

(1) The sequence is written such that no state repeats itself. The binary sequence is repeated once in every 2^{N-1} clock cycles.

(2) The Expression for 'f ' is got using K-map.

(3) Rig up the circuit as shown in the figure.

(4) Initially let M = 1, clkp = $c_{p,}$ the initial state (A, B, C, D -1111) is loaded.

(5) Then make clks =C_p, M = 0, output is observed at MSB (A).

Note: When we observe the sequence, which is to be generated, the LSB is a 1, following bit is 0. If 0 has to be generated, then input to that particular D-Flip Flop must be a 0. Therefore f(Q_A, Q_B, Q_C, Q_D) has its first entry as 0.

Conclusion:

EXPERIMENT NO 12

Mod-N Counter

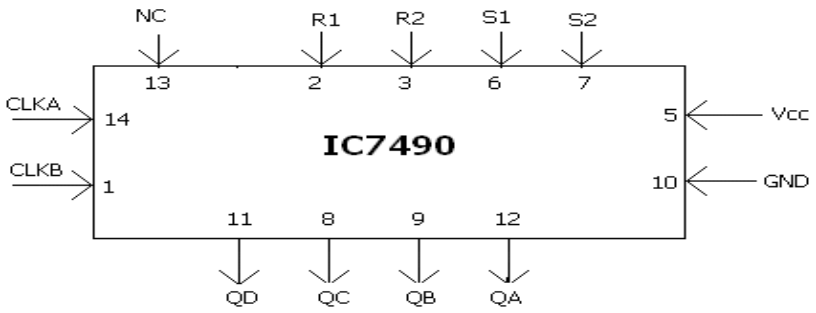
Aim: Realization of 3-bit counters as a sequential circuit and mod-N counter design using 7476, 7490, 74192, 74193.

Components Required:

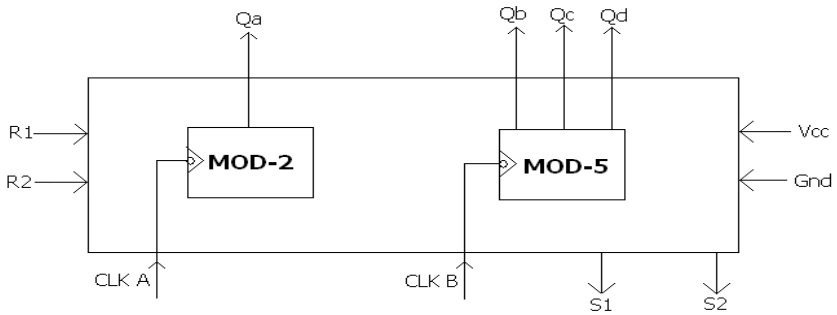
Sl.No	Name of the Component	IC Number	Qty
1	Decade Counter	7490	1
2	Programmable 4-bit Sync up/down decade Counter	74192	1
3	Programmable 4-bit Sync up/down Counter	74193	1
4	Patch chords		few
5	Trainer Kit		

To realize a MOD-N counter using IC-7490

PIN DIAGRAM



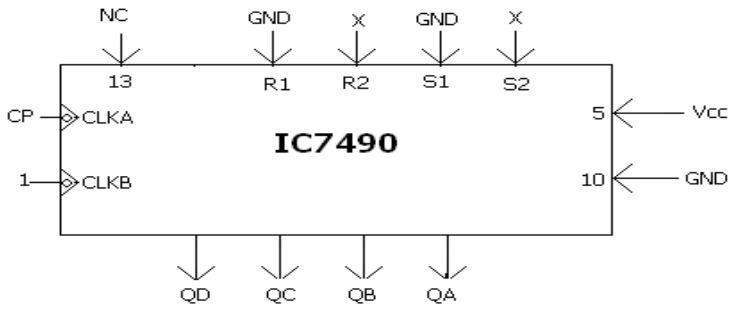
INTERNAL DIAGRAM



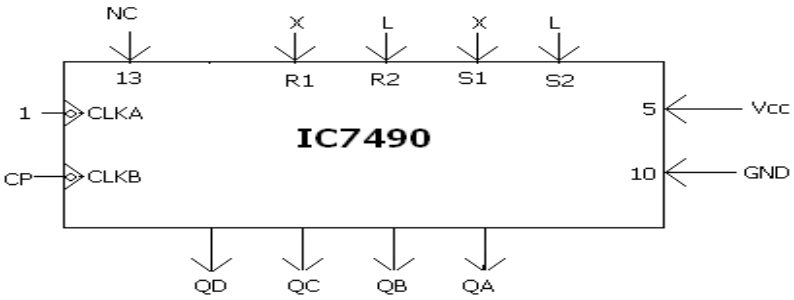
Functional Table

Inputs				Outputs			
R1	R2	S1	S2	Qa	Qb	Qc	Qd
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	L	H	H	1	0	0	1
L	X	L	X	MOD-2 COUNTER			
X	L	X	L	MOD-5 COUNTER			

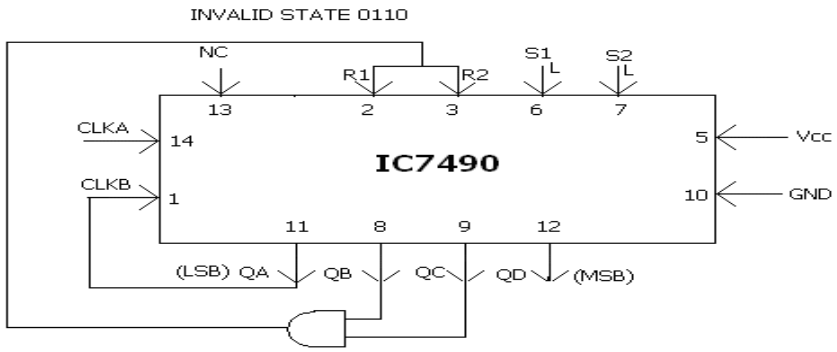
7490 AS MOD-2 COUNTER



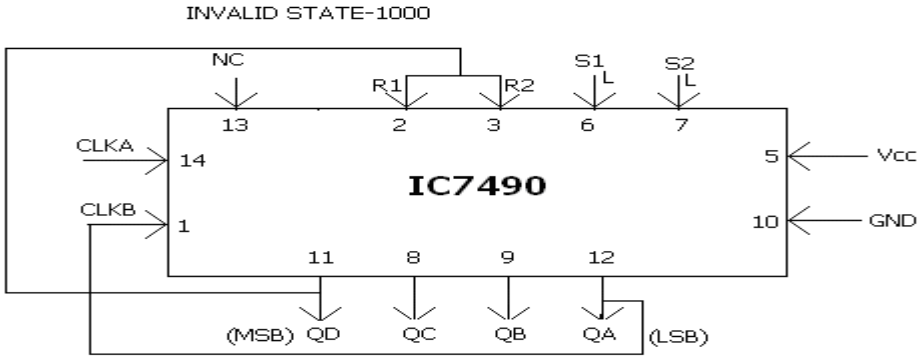
7490 AS MOD-5 COUNTER



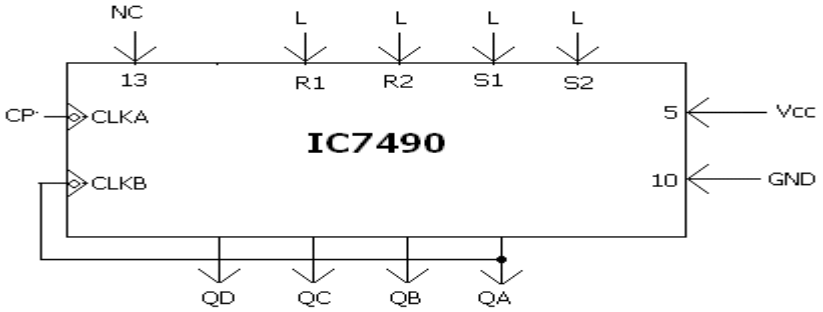
7490 AS MOD-6 COUNTER



7490 AS MOD-8 COUNTER



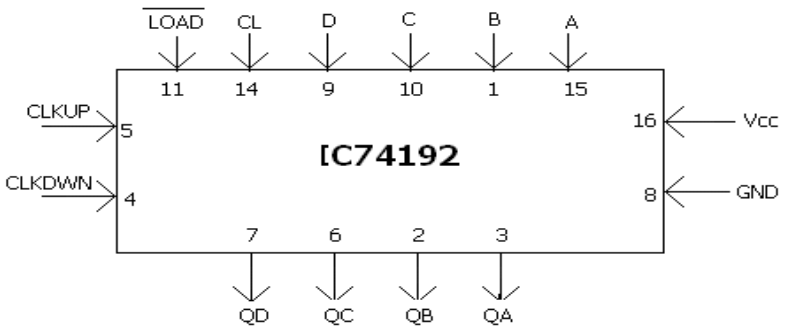
7490 AS MOD-10 COUNTER



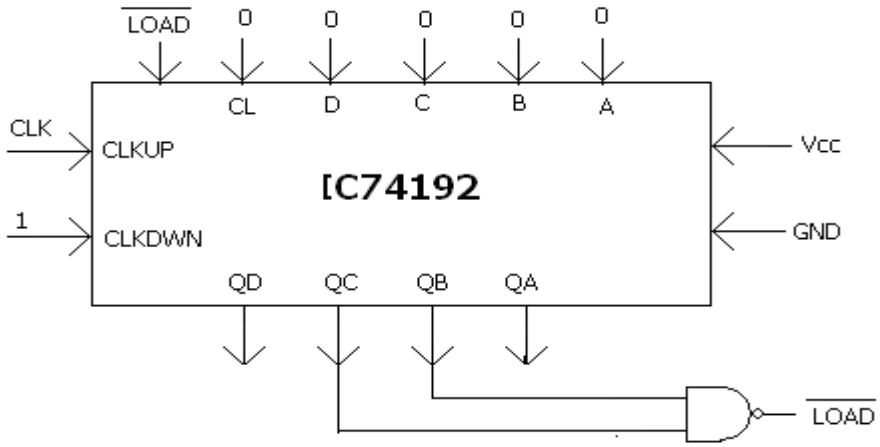
Procedure:

1. Connections are as per the logic diagram.
2. Inputs are applied at R1, R2, S1 & S2.
3. Apply clock pulses one by one and verify the truth table**.**

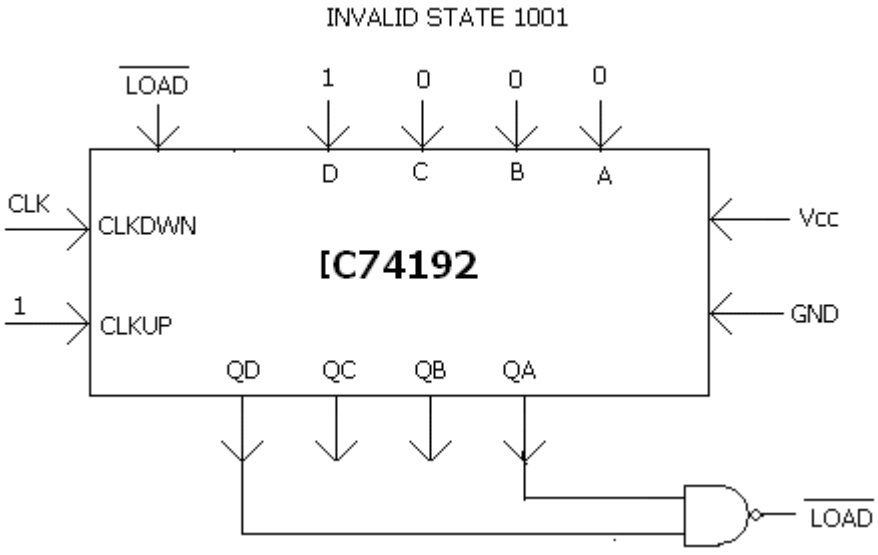
PIN DETAILS OF IC-74192



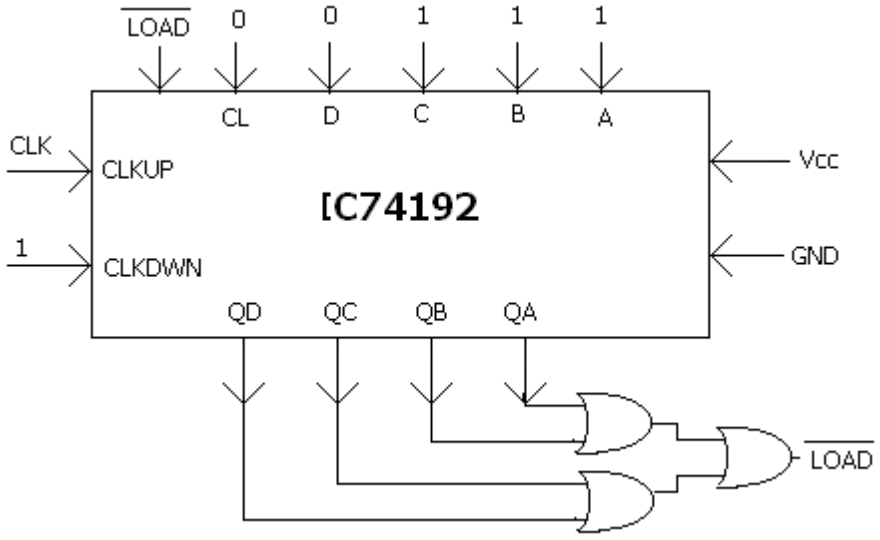
MOD-6 UP COUNTER: Invalid state o110



MOD-9 DOWN COUNTER:



DESIGN A COUNTER WHICH CAN COUNT FROM 7 TO 9



NOTE After 1001, output becomes 0000

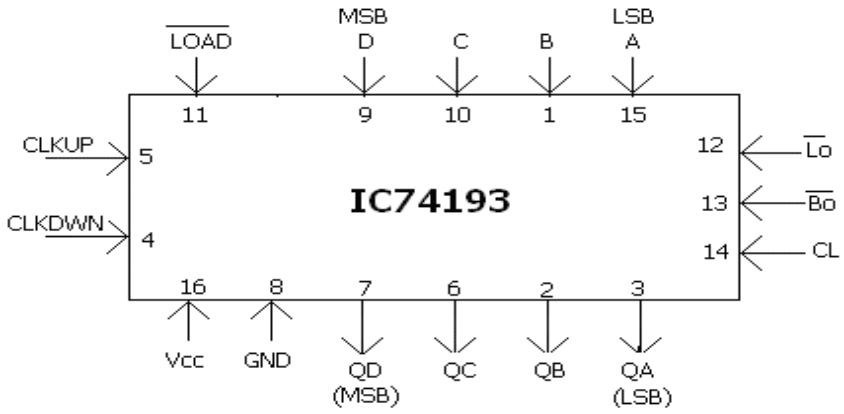
Procedure:

1. Connections are made as shown in the logic diagram with load pin open.
2. The present value is made available at the data inputs A, B, C and D.
3. The load pin is made low so that the present value appears at Qd, Qc, Qb and Qa.
4. The output of the gate is then connected to the load input.
5. Clock pulses are applied one by one and the truth table is verified.

MOD-N COUNTERS

To realize a MOD-N counter using IC-74193 with a given preset value, write down the expected function table

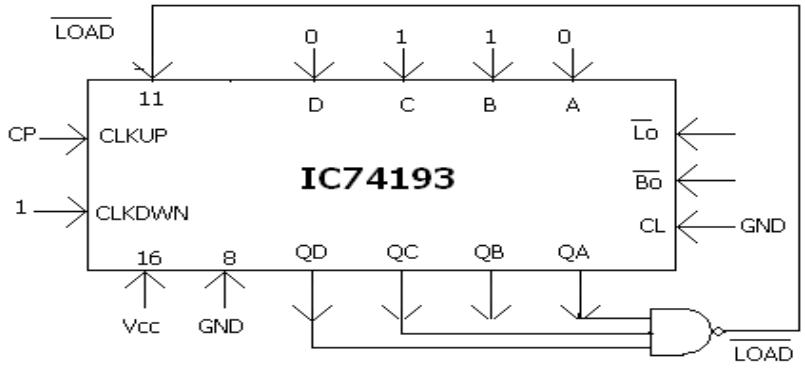
Pin details of IC 74193(Synchronous counter)



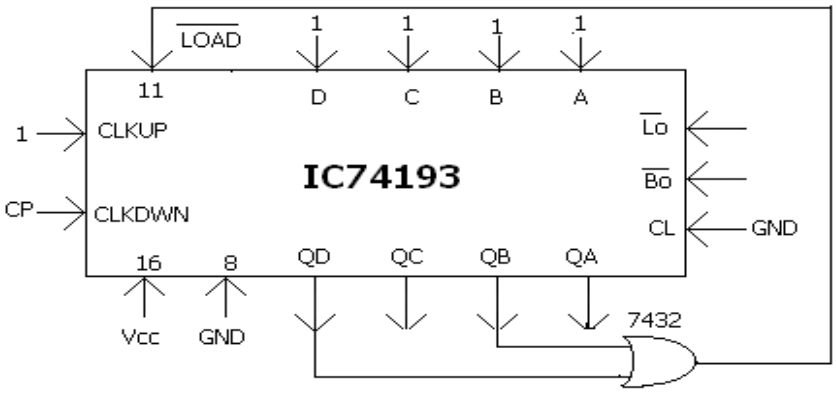
FUNCTION TABLE

Inputs				Outputs			
Clr'	Load	Up	Down	Q_d	Q_c	Q_b	Q_a
H	X	X	X	0	0	0	0
L	L	X	X	D	C	B	A
L	H	Cp	H	COUNT UP			
L	H	H	Cp	COUNT DOWN			
L	H	H	H	NO CHANGE			

Design a counter which counts from (6-12) Invalid state 1101



REALIZE A (15-6) COUNTER USING IC 74193



Invalid state---0101

Note:-Lo and Bo are used basically for cascading the counters

Procedure:

1. Connections are made as shown in the logic diagram with load pin open.
2. The present value is made available at the data inputs A, B, C and D.
3. The load pin is made low so that the present value appears at Qd, Qc, Qb and Qa.
4. The output of the gate is then connected to the load input.
5. Clock pulses are applied one by one and the truth table is verified.

Conclusion:

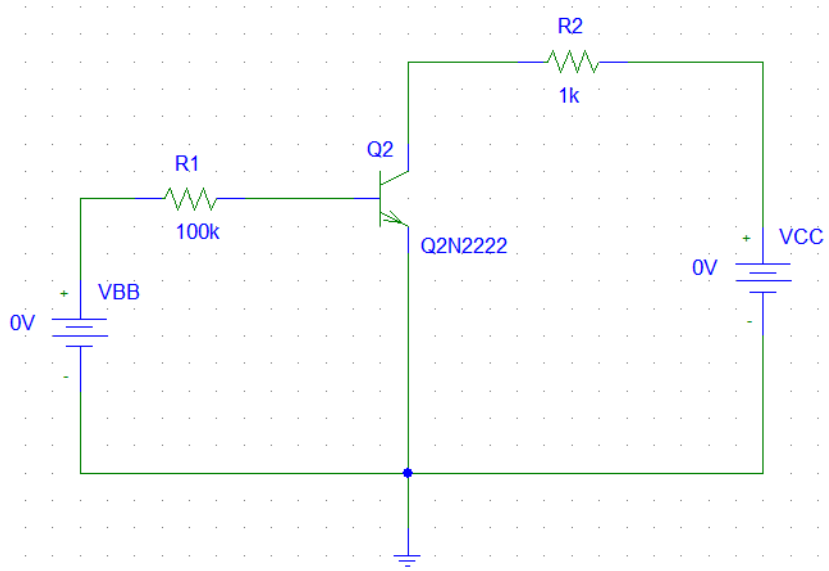
Simulation Experiments

AIM: Simulation of Input and Output characteristics of NPN transistor in Common Emitter Configuration.

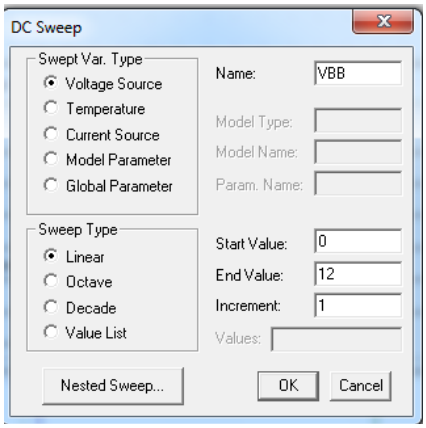
PROCEDURE:

(For Schematics)

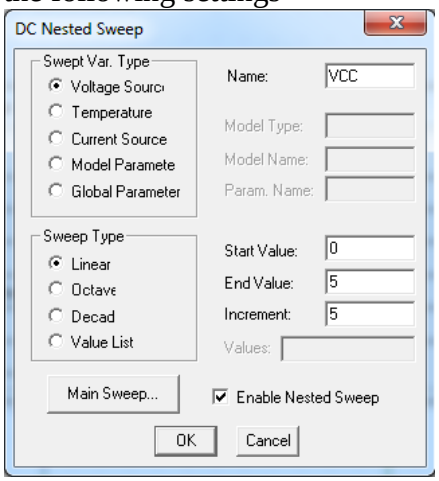
1. Double click on Pspice icon.
2. Go to File menu & click on New.
3. Draw the following circuit. For that go to Get New Part menu. Select the components that you need. Connect with wire.



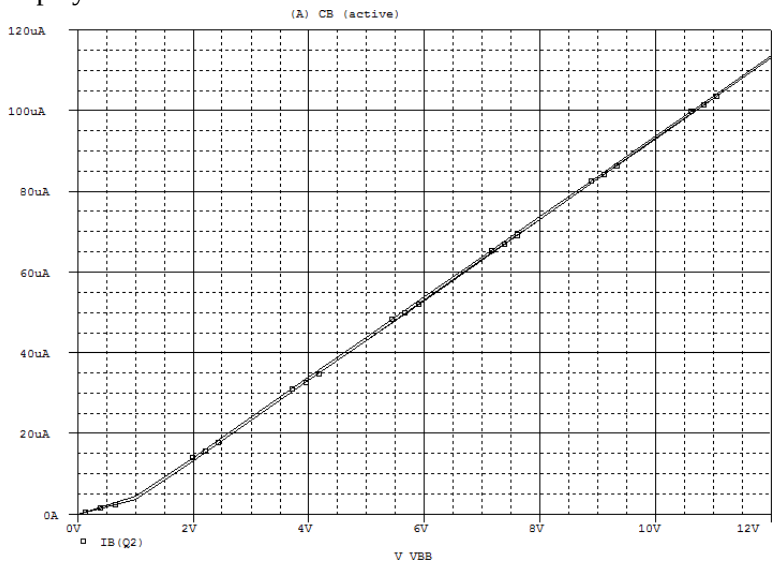
4. Go to Setup Analysis tick Bias Point Detail, DC sweep option. In DC sweep option do the following settings



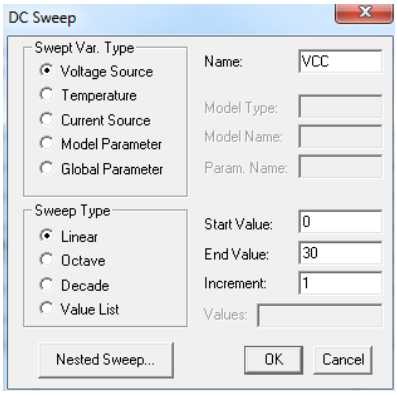
Now click on Nested Sweep and do the following settings



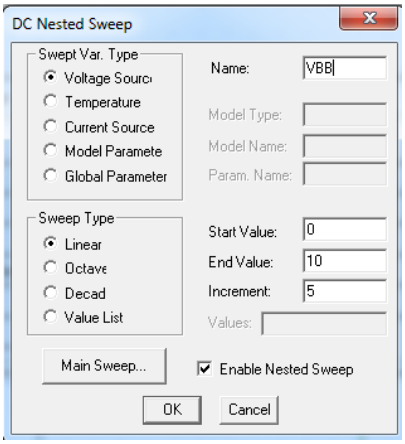
5. Now click on Simulate. In simulation window click on Add Trace and select IB(Q2) and click OK. The Input characteristics will be displayed.



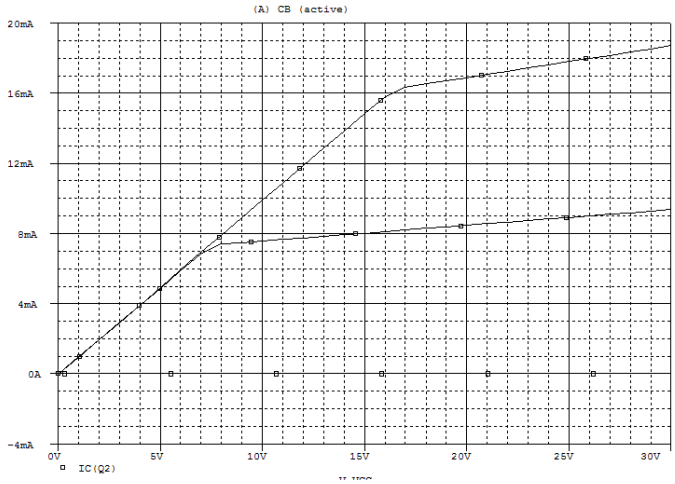
6. Go to Setup Analysis tick Bias Point Detail, DC sweep option. In DC sweep option do the following settings



Now click on Nested Sweep and do the following settings



7. Now click on Simulate. In simulation window click on Add Trace and select IC(Q2) and click OK. The Output characteristics will be displayed.

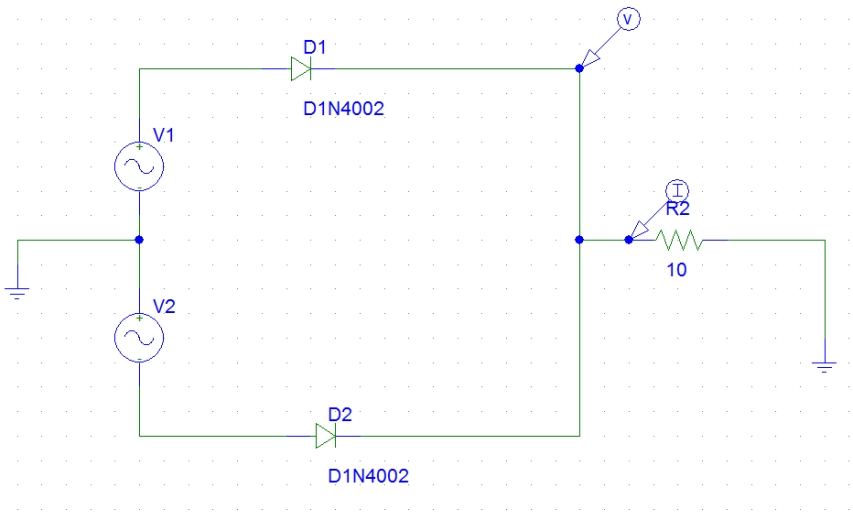


AIM: Simulation of Centre tap full wave rectifier.

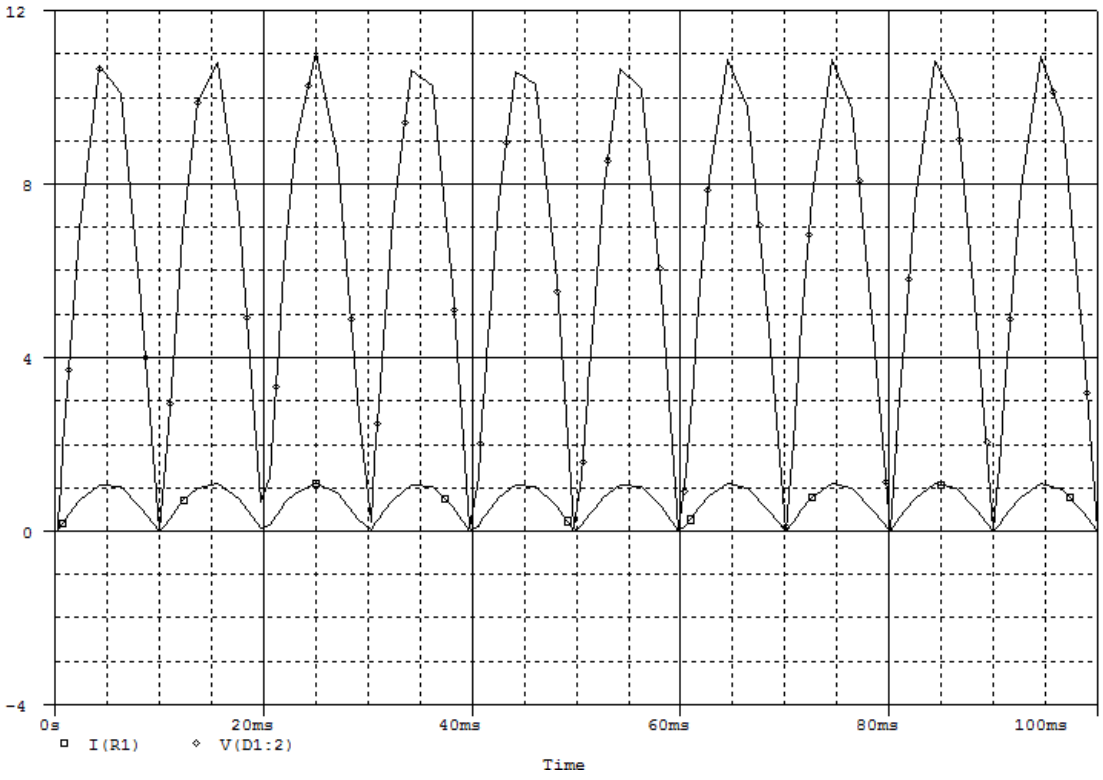
PROCEDURE:

(For Schematics)

1. Double click on Pspice icon.
2. Go to File menu & click on New.
3. Draw the following circuit. For that go to Get New Part menu. Select the components that you need. Connect with wire. Connect the voltage and current marker.



4. Now double click on VSIN symbol and set the following values DC=0, AC=0, VOFF=0, VAMPL=12v, FREQ=50. For R1 set VALUE=10.
5. Go to Setup Analysis menu and tick the option Bias Point Detail and Transient. In the Transient option set the Final Time at 100ms.
6. Now click on Simulate. The output voltage and current waveform will be displayed.

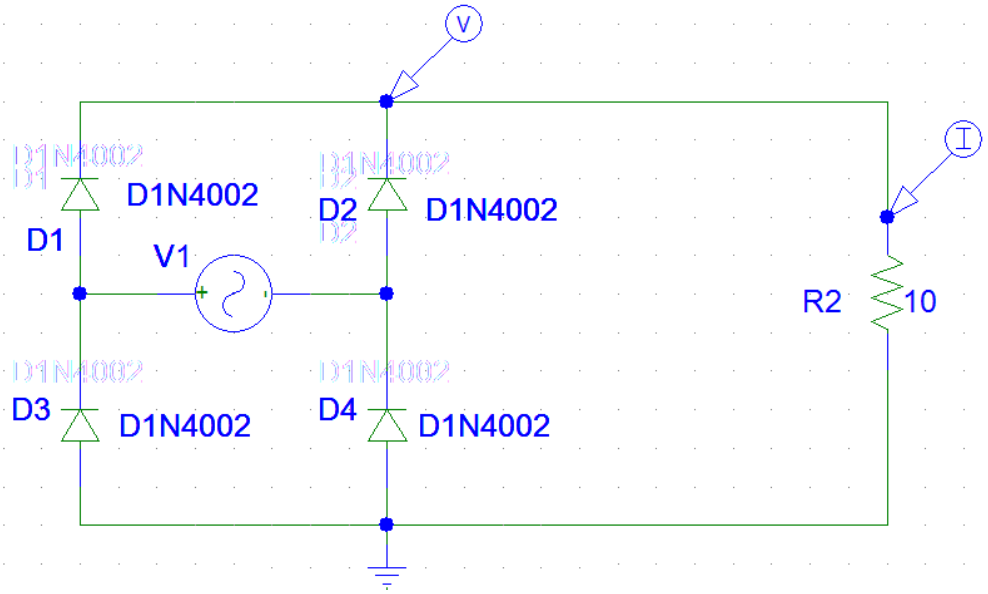


AIM: Simulation of Full wave bridge rectifier.

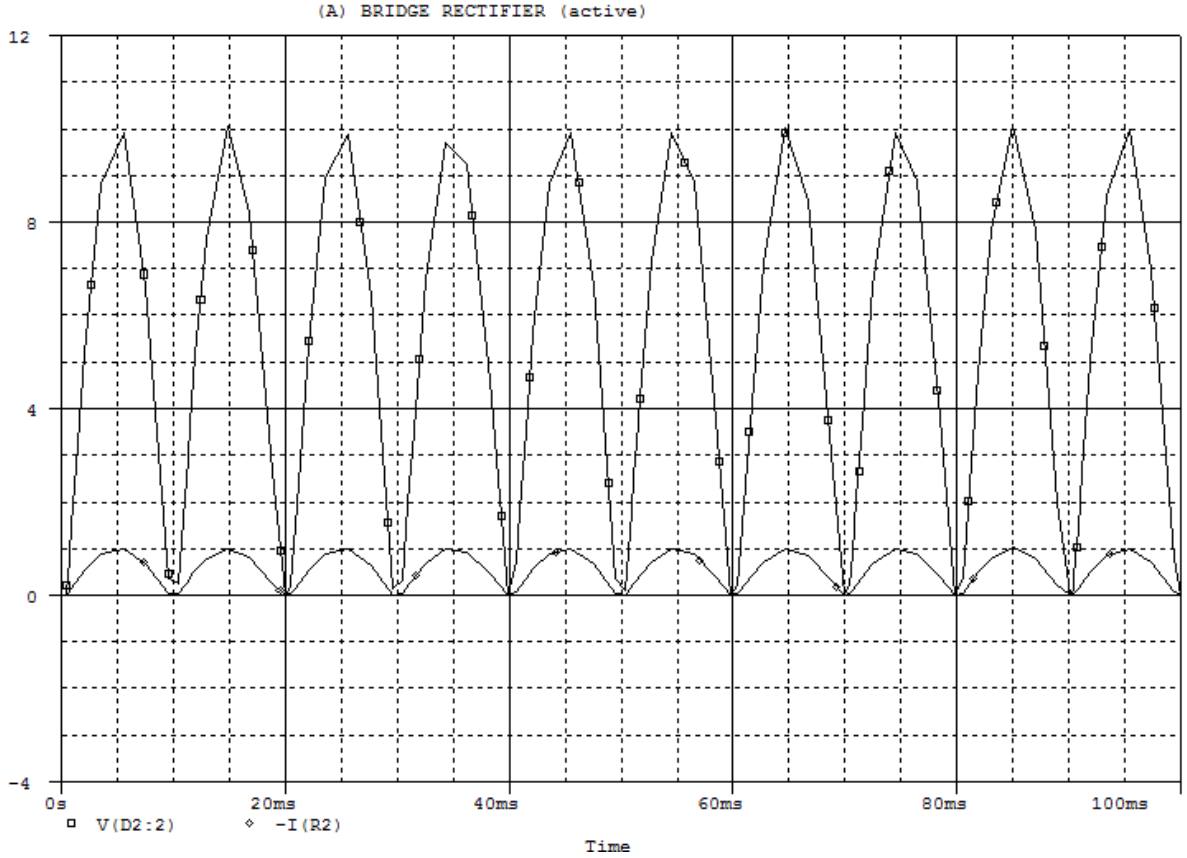
PROCEDURE:

(For Schematics)

1. Double click on Pspice icon.
2. Go to File menu & click on New.
3. Draw the following circuit. For that go to Get New Part menu. Select the components that you need. Connect with wire. Connect the voltage and current marker.



4. Now double click on VSIN symbol and set the following values DC=0, AC=0, VOFF=0, VAMPL=12v, FREQ=50. For R1 set VALUE=10.
5. Go to Setup Analysis menu and tick the option Bias Point Detail and Transient. In the Transient option set the Final Time at 100ms.
6. Now click on Simulate. The output voltage and current waveform will be displayed.

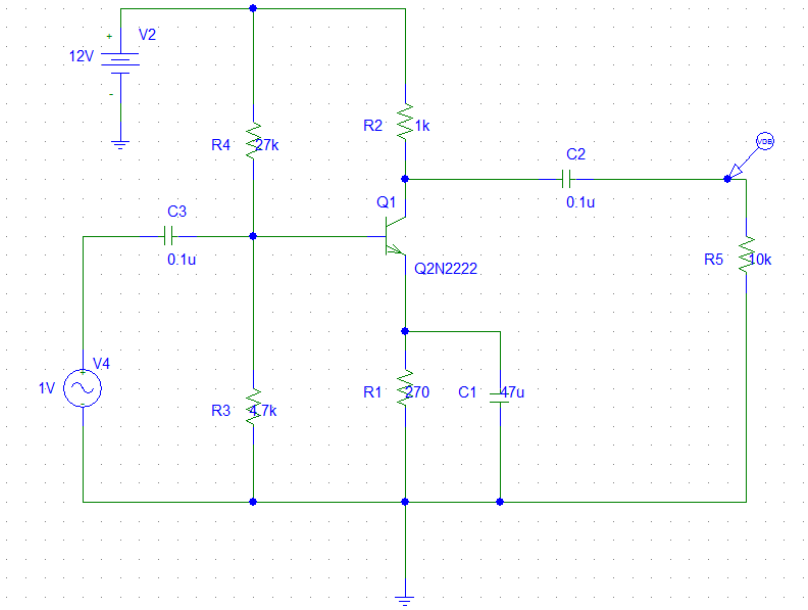


AIM: Simulation of RC coupled amplifier.

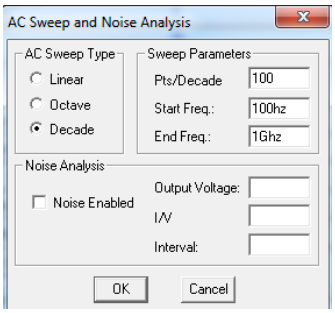
PROCEDURE:

(For Schematics)

1. Double click on Pspice icon.
2. Go to File menu & click on New.
3. Draw the following circuit. For that go to Get New Part menu. Select the components that you need. Connect with wire. Connect the VDB marker.



4. Now double click on VAC symbol and set the following values ACMAG=1V.
5. Go to Setup Analysis menu and tick the option Bias Point Detail, Transient and AC Sweep. In the AC Sweep option do the following settings and click OK.



In the Transient option set the Print setup 0ms and Final Time at 30ms and click OK.

6. Now click on Simulate and select the Analysis type AC. The frequency response will be displayed.