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DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Operational Amplifier & Linear ICs

Laboratory Manual

18EEL48

Faculty Incharge

Prof. K. B. Negalur & Prof. S. S. Birade

DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

VISION

“To be the centre of excellence in teaching and learning to produce the competent & socially responsible professionals in the domain of Electrical & Electronics Engineering.”

MISSION

- I. To educate students with core knowledge of Electrical and Electronics Engineering to excel in their professional career.
- II. To develop problem solving skills, professional skills and ethical values among the students for the betterment of mankind.
- III. To prepare technically competent and socially responsible Electrical Engineer to serve the future needs of the society.

Program Educational Objectives (PEOs):

Engineering Graduates will be able to:

- PEO1:** Achieve successful professional career in Electrical Engineering and allied disciplines.
- PEO2:** Pursue higher studies and continuously engage in upgrading the professional skills.
- PEO3:** Demonstrate professional & ethical values, effective communication skills and teamwork to solve issues related to profession, society and environment.

Program Specific Outcomes (PSOs):

Engineering Graduates will be able to:

- PSO1:** Apply knowledge & competencies to analyze & design Electrical & Electronics circuits, control and power systems, machines & industrial drives.
- PSO2:** Use software/hardware tools for the design, simulation and analysis of Electrical and Electronics Systems.



Overview

Year / Semester	2 nd Year /4 th Semester	Academic Year	2021-22
Laboratory Title	Op-Amp & Linear ICs Lab	Laboratory Code	18EEL48
Total Contact Hours	42 Hours	Duration of SEE	3 Hours
IA Marks	40 Marks	SEE Marks	60 Marks

Objectives

- To conduct different experiments using OP-Amps
- To conduct experiments using Linear IC's

Description

1.0 Learning Objectives

Student aims to understand, design and analyze the basic applications of the linear IC, mainly the op-amp. In this laboratory student designs many circuits namely inverting, non-inverting mode of op-amp, adder circuit, subtractor, integrator, R-2R DAC, voltage comparator etc.

2.0 Learning Outcomes

The student, after successful completion of the course, will be able to

1. To conduct experiment to determine the characteristic parameters of Op-Amp.
2. To design the Op-Amp as Amplifier, adder, subtractor, differentiator & integrator
3. To design test the OP-Amp as oscillators and filters.
4. Design and study of Linear IC's as multivibrator power supplies.

Prerequisites

- Basic knowledge of bread board connection methods.
- Details of various elements like pin configuration of IC 741, colour code of resistors etc.
- Analog Electronic Circuits design and analysis

Base Course

1. Analog Electronic Circuits.
2. Operational Amplifiers & Linear Integrated Circuits.

Introduction

In Op-amp and linear IC lab we are conducting experiments using op-amp IC 741 such as op-amp operation mode namely inverting and non-inverting mode also some applications of op-amps are also designed and analyzed practically like adder, subtractor, integrator, differentiator, Schmitt trigger etc. At the end of the course student will be able to understand and design op-amp circuits and get the performance practically.

Resources Required

1. Signal Generator
2. Dual Power Supply
3. Bread Boards
4. ICs like 741, 79**, 78**, 555 timer ec
5. Digital Storage Oscilloscope



General Instructions

1. After circuit connection, before switching ON the supply, verify it by instructor or lab in charge.
2. Make sure voltage level of dual supply is at minimum value at the start.
3. Before leaving the lab keep all the equipments properly.

Contents

Expt No.	Title of the Experiment	Date Planned	Date Conducted
1	Design and verify a precision full wave rectifier. Determine the performance parameters.		
2	Design and realize to analyze the frequency response of an op – amp amplifier under inverting and non - inverting configuration for a given gain.		
3	Design and verify the output waveform of an op – amp RC phase shift oscillator for a desired frequency		
4	Design and realize Schmitt trigger circuit using an op – amp for desired upper trip point (UTP) and lower trip point (LTP).		
5	Verify the operation of an op – amp as (a) voltage comparator circuit and (b) zero crossing detector.		
6	Design and verify the operation of op – amp as an (a) adder (b) subtractor (c) integrator and (d) differentiator.		
7	Design and realize an op – amp based first order Butterworth (a) low pass (b) high pass and (c) band pass filters for a given cut off frequency/frequencies to verify the frequency response characteristic.		
8	Design and realize an op – amp based function generator to generate sine, square and triangular waves of desired frequency.		
9	Design and realization of R – 2R ladder DAC.		
10	Realization of Two bit Flash ADC		
11	Design and verify an IC 555 timer based pulse generator for the specified pulse.		
12	Designing of Fixed voltage power supply (voltage regulator) using IC regulators 78 series and 79 series		

Evaluation Scheme

1. Lab activity – Continuous Assessment – 30 Marks.
2. Internal exam at the end of semester – 10 Marks.
3. Semester End Exam – 100 Marks. (Scaled down to 60 Marks.)

Reference

- Operational Amplifiers & Linear ICs, David A. Bell, Oxford University Press 3rd Edition 2011.
- Operational Amplifiers: Theory and Practice Second Edition Version 1.8.1 James K. Roberge Kent H. Lundberg Massachusetts Institute of Technology April 19, 2007



Experiments

1.0 PRECISION RECTIFIER

Experiment No	Date Planed	Date Conducted	Marks
01			

1.1 Learning Objectives

1. Rectification operation using op-amp.
2. Can conclude that the rectifier circuit designed by using op-amp is more precise than that of diode circuit.

1.2 Aim

Design and verify a precision full wave rectifier. Determine the performance parameters.

1.3 Equipment Required

Sl No	Element	Range	Quantity
1	Op-amp	741 IC	02
2	Diode	IN4007	02
3	Resistors	10K Ω , 20K Ω	05,01
4	Function Generator	0.1-1 MHz	01
5	Potentiometer	50k Ω	01
6	Regulated Power supply	0-30 V 1A	01
7	Cathode Ray Oscilloscope	0 -20MHz	01

1.4 Theory

The use of Operational amplifiers can improve the performance of a wide variety of signal processing circuits. In rectifier circuits, the voltage drop that occurs with an ordinary semiconductor rectifier can be eliminated to give precision rectification.

The below shown circuit is the precision full wave rectifier. It consists of following sections:

1. Precision half-wave rectifier
2. Inverting summing amplifier

The input voltage V_{in} is applied to one terminal of the summing amplifier along with resistor R3 and to the input of the precision rectifier. The output of precision rectifier is applied to another terminal of summing amplifier. The precision half-wave rectifier circuit uses an inverting amplifier configuration.

1.5 Procedure

1. Connections are made as per the circuit diagram shown in fig 1.
2. Apply sinusoidal input of 0.5V peak to peak at the inverting terminal of the op-amp.
3. Note down the output voltage and observe the direction of the output on the CRO.
4. Calculate the output voltage and the gain of the circuit.
5. Draw the graph.



1.6 Circuit Diagram

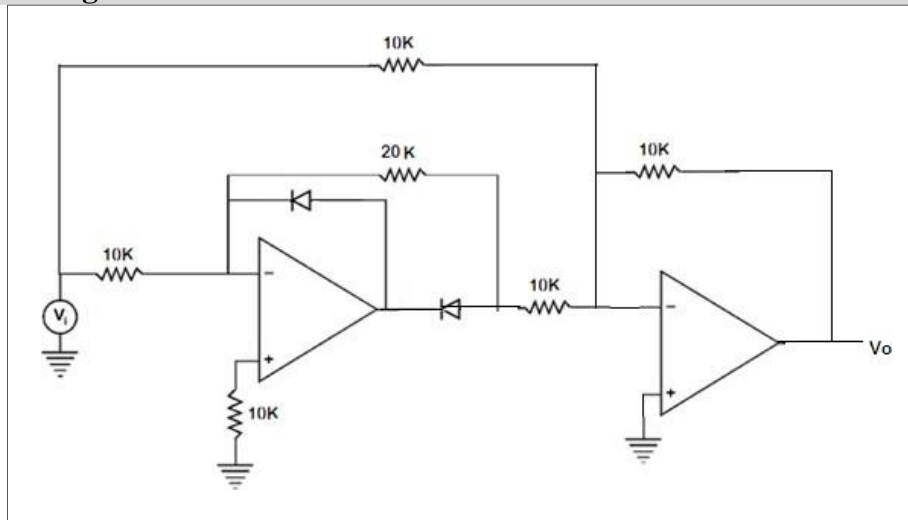


Fig 1. Precision full wave rectifier circuit

1.7 Observation Table

Peak to Peak Input Voltage V_{p-p} = _____

Time Period T = _____

Output voltage V_o = _____

1.8 Formula / Calculations

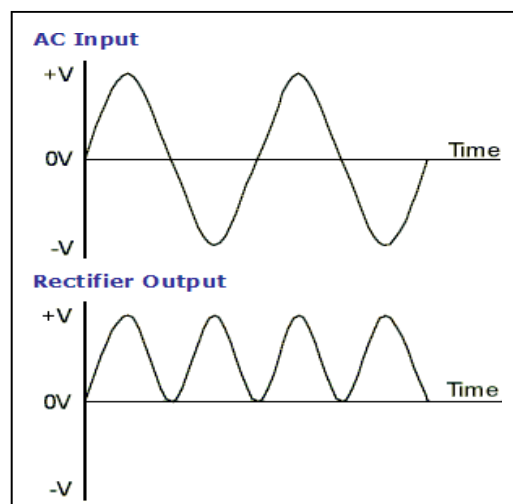
DESIGN

The gain of precision half wave rectifier should be exactly equal to 2 so we choose $R_2 = 2R_1$

Therefore, let us choose $R_1 = 10\text{Kohm}$

And $R_2 = 20\text{Kohm}$

1.9 Outputs





1.10 Results & Analysis

1.11 Outcome & Conclusion

1.12 Remarks

Faculty Signature



Experiments

2.0 INVERTING & NON-INVERTING AMPLIFIERS

Experiment No	Date Planed	Date Conducted	Marks
02			

2.1 Learning Objectives

1. Student will be able to identify the mode of operation of the op-amp.
2. Can analyze the op-amp circuits by studying the output waveforms.

2.2 Aim

Design and realize to analyze the frequency response of an op-amp amplifier under inverting and non - inverting configuration for a given gain.

2.3 Equipment Required

SI No	Element	Range	Quantity
1	Op-Amp	IC741	01
2	Function Generator	0.1-10Mhz	01
3	Resistor	1K Ω ,10K Ω	01 each
4	CRO		01
5	Regulated Power Supply Dual	\pm 12V	01
6	Bread Board		01
7	Connecting Leads		Few

2.4 Theory

Inverting Amplifier:

The input signal V_i is applied to the inverting input terminal through R_1 and the non-inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the $R_f - R_1$ network, where R_f is the feedback resistor. The output voltage is given as,

$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is 180° out of phase with the input signal.

Non-Inverting Amplifier:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

$$V_o = A_{CL} V_i$$

Here the output voltage is in phase with the input signal.



2.5 Procedure

Inverting

1. Connections are made as per the circuit diagram.
2. + V_{CC} and - V_{CC} supply is given to pin no 7 and 4 of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp. (5V p-p, 1 KHz)
4. The output voltage is obtained on the CRO and the input and output voltage waveforms are plotted in a graph sheet.

Non-Inverting

1. Connections are given as per the circuit diagram.
2. + V_{CC} and - V_{CC} supply is given to the power supply terminals of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp. (5V p-p, 1 KHz)
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

2.6 Circuit Diagram

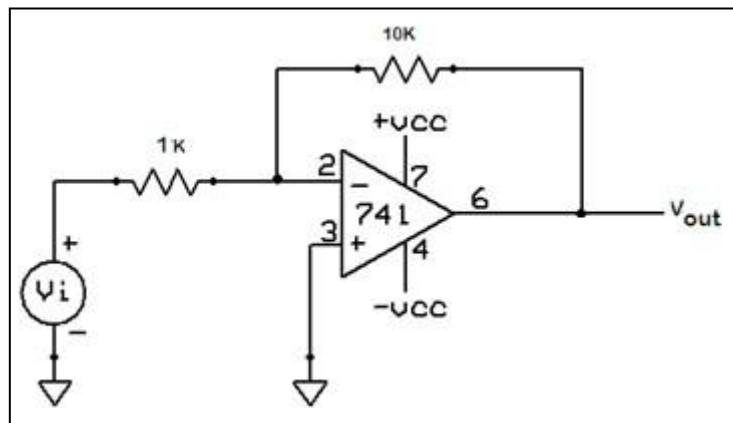


Fig 1. Inverting Amplifier Circuit

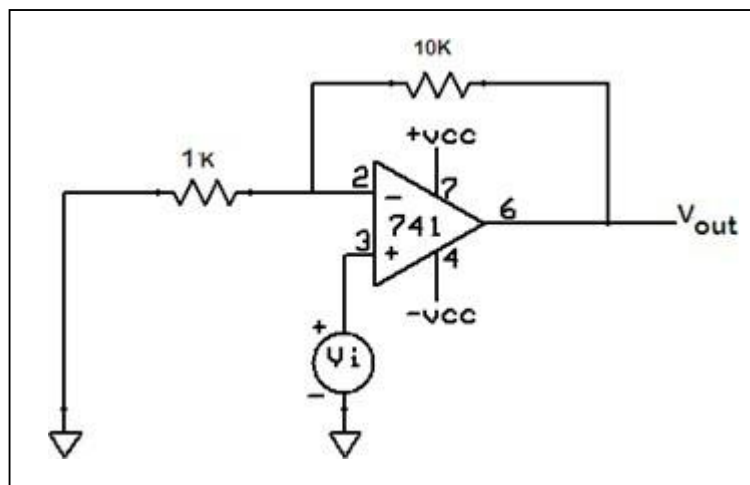


Fig 2. Non-Inverting Amplifier Circuit



2.7 Observations

A. Inverting amplifier

Sl No	Frequency in Hz	Output Voltage	Gain V_o/V_i	Gain in dB
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

B. Non Inverting Amplifier

Sl No	Frequency in Hz	Output Voltage	Gain V_o/V_i	Gain in dB
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

2.8 Formula

We know for an inverting Amplifier $A_{CL} = R_F / R_1$
 Assume R_1 (approx. 10 K Ω) and find R_F
 Hence $V_o = - A_{CL} V_i$

We know for a Non-inverting Amplifier $A_{CL} = 1 + (R_F / R_1)$
 Assume R_1 (approx. 10 K Ω) and find R_F
 Hence $V_o = A_{CL} V_i$

2.9 Outputs

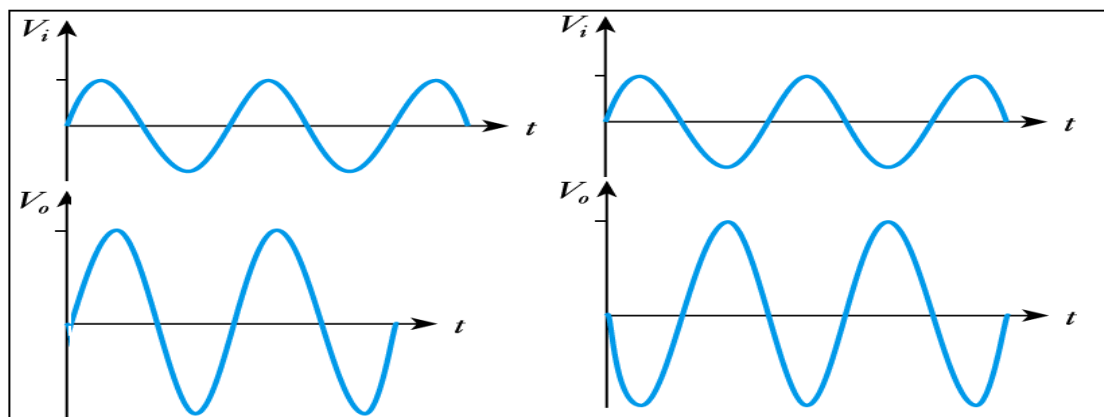


Fig 3 Output Waveforms a) Non-Inverting Amplifier b) Inverting Amplifier



2.10 Results & Analysis

2.11 Outcome & Conclusion

2.12 Remarks

Faculty Signature



Experiments

3.0 RC PHASE SHIFT OSCILLATOR

Experiment No	Date Planed	Date Conducted	Marks
03			

3.1 Learning Objectives

1. Student will study how 180 degree phase shift is achieved by op-amp.
2. Generation of sine wave by using op-amp as oscillator circuit.

3.2 Aim

Design and verify the output waveform of an op – amp RC phase shift oscillator for a desired frequency.

3.3 Equipment Required

Sl No	Element	Range	Quantity
1	Op-amp	IC- 741	01
2	Resistors	1.2K Ω 1 K Ω	01 02
3	Capacitor	0.01 μ f	03
4	Potentiometer	50K Ω	01
5	Regulated Power supply	(Dual) 0 – 30V	01
6	CRO	0 – 20MHz	01
7	Bread Board		01

3.4 Theory

RC phase shift oscillator is a sinusoidal oscillator used to produce sustained well shaped sine wave oscillations. It is used for different applications such as local oscillator for synchronous receivers, musical instruments, study purposes etc. The main part of an RC phase shift oscillator is an op amp inverting amplifier with its output fed back into its input using a regenerative feedback RC filter network.

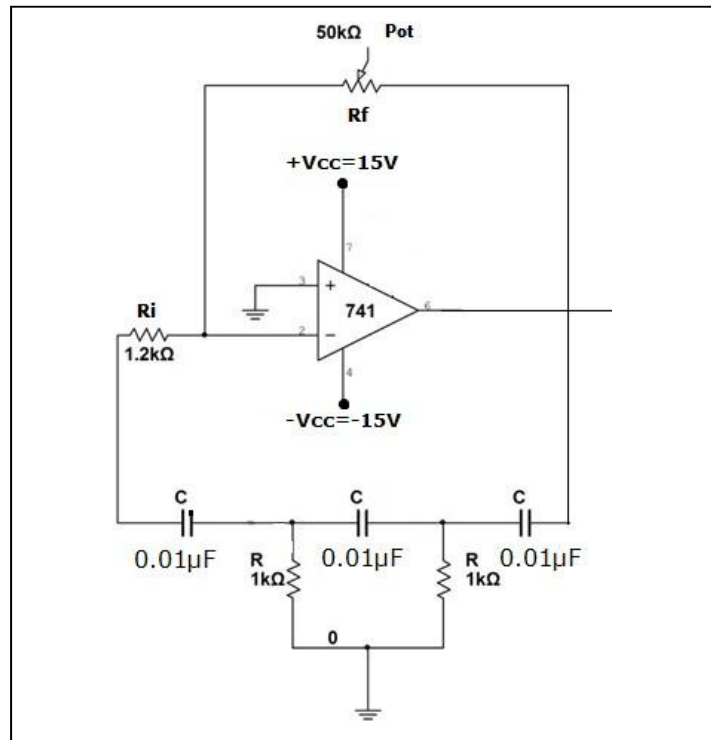
Basically, positive feedback of a fraction of output voltage of a amplifier fed to the input in the same phase, generate sine wave. The op-amp provides a phase shift of 180° as it is used in the inverting mode. An additional phase shift of 180 degree is provided by the feedback RC network. The feedback network consists of 3 RC sections producing each 60° phase shift. Such a circuit is known as RC phase shift network.



3.5 Procedure

1. Connect the circuit as shown in fig. With the design values.
2. Observe the output waveforms using a CRO. For obtaining sine wave adjust R_f .
3. Measure the output wave frequency and amplitude.

3.6 Circuit Diagram



3.7 Observation Table

Time period =

Frequency =

Amplitude =

3.8 Formula / Calculations

Frequency of oscillation (F):

$$F = \frac{1}{2\pi RC\sqrt{6}}$$

$$\text{so for } 6.5\text{kHz} = \frac{1}{2\pi \times 1000 \times 0.01 \times 10^{-6} \times \sqrt{6}}$$



Gain of the Op Amp inverting amplifier (G):

$$G = -\frac{R_f}{R_i} = 29$$

Attenuation offered by the feedback RC network is 1/29, so the gain of inverting amplifier should be 29

Use $R_i = 1.2 \text{ K}\Omega$

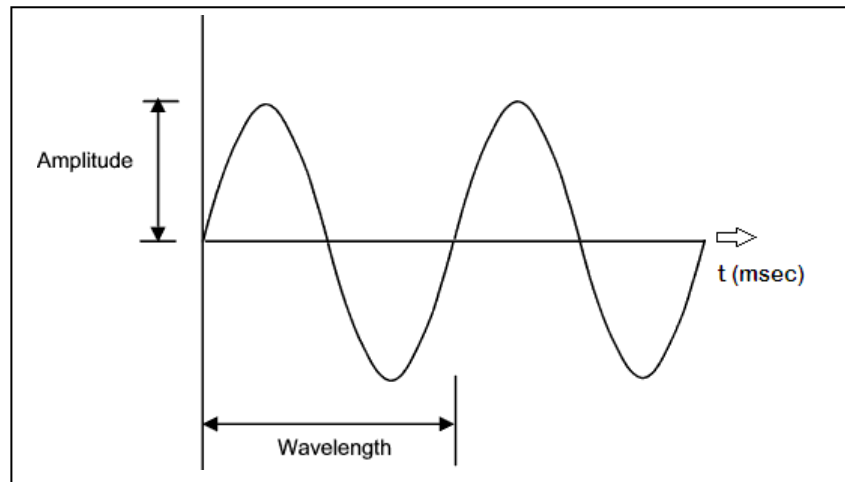
So, $R_f = 35 \text{ K}\Omega$

Use 50K Ω potentiometer and adjust its value to obtain output on CRO

The frequency of the oscillator f_0 is given by

$$f_0 = 1 / (2\pi RC) \sqrt{6}$$

3.9 Outputs



3.10 Results & Analysis

3.11 Outcome & Conclusion

3.12 Remarks

Faculty Signature



Experiments

4.0 SCHMITT TRIGGER

Experiment No	Date Planed	Date Conducted	Marks
04			

4.1 Learning Objectives

1. For different UTP and LTP values circuit can be designed.
2. Study the Schmitt Trigger operation.

4.2 Aim

To design and realize Schmitt trigger circuit using an op – amp for desired upper trip point (UTP) and lower trip point (LTP).

4.3 Equipment Required

Sl No	Element	Range	Quantity
1	Op-Amp	IC- 741	01
2	Resistors	1 K Ω 10 K Ω	02 01
3	CRO/DSO	0-20MHz	01
4	Bread Board		01
5	Signal Generator	0.1-1MHz	01
6	Dual Power Supply	+/-12 V	01
7	Multimeter		01
8	Connecting wires		Few

4.4 Theory

Schmitt Trigger is also known as Regenerative Comparator. This is a square wave generator which generates a square based on the positive feedback applied. As shown in the fig. below, the feedback voltage is V_a . The input voltage is applied to the inverting terminal and the feedback voltage is applied to the non-inverting terminal. In this circuit the op-amp acts as a comparator. It compares the potentials at two input terminals. Here the output shifts between + V_{sat} and - V_{sat} . When the input voltage is greater than V_a , the output shifts to - V_{sat} and when the input voltage is less than V_a , the output shifts to + V_{sat} . Such a comparator circuit exhibits a curve known as Hysteresis curve which is a plot of V_{in} Vs V_0 . The input voltage at which the output changes from + V_{sat} to - V_{sat} is called Upper Threshold Point (UTP) and the input voltage at which the output shifts from - V_{sat} to + V_{sat} is called Lower Threshold Point (LTP). The feedback voltage V_a depends on the output voltage as well as the reference voltage. A Zero Cross Detector is also a comparator where op-amp compares the input voltage with the ground level. The output is a square wave and inverted form of the input.



4.5 Procedure

1. Connect the circuit as shown in Fig 1.
2. Apply sine/triangular waveform of peak voltage greater than UTP.
3. Observe the output at pin 6 of the IC 741, vary the input and note down the readings.
4. Find the upper and lower threshold voltages (UTP, LTP) from the output wave form.

4.6 Circuit Diagram

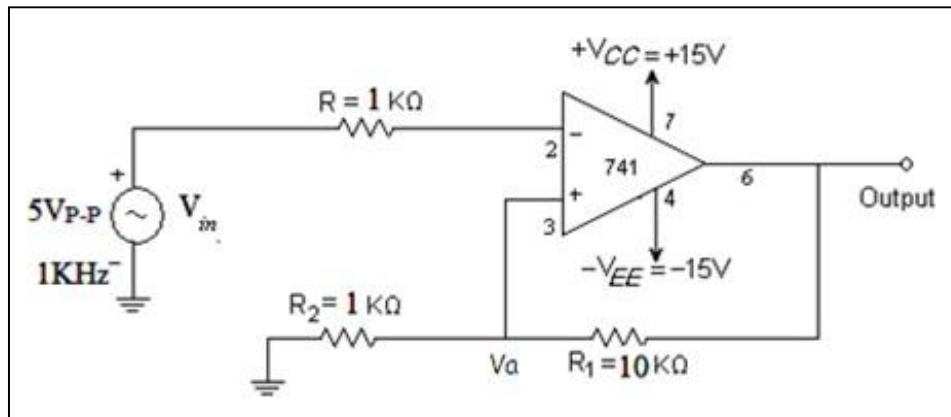


Fig 1. Schmitt Trigger Circuit

4.7 Observation Table

Parameter	Theoretical Value	Practical Value
UTP		
LTP		

4.8 Formula / Calculations

Given UTP = + 4V and LTP = - 2V

Let I₁ be the current through R₁ and I₂ be the current through R₂.

W.K.T the current into the input terminal of an op-amp is zero.

$$I_1 + I_2 = 0$$

$$I_1 = (V_0 - V_a) / R_1$$

$$\text{similarly } I_2 = (V_{ref} - V_a) / R_2$$

$$(V_0 - V_a) / R_1 + (V_{ref} - V_a) / R_2 = 0$$

$$V_a = (V_0 R_2 + V_{ref} R_1) / (R_1 + R_2)$$

$$\text{When } V_0 = + V_{sat}, V_a = \text{UTP}$$

$$\text{\& When } V_0 = - V_{sat}, V_a = \text{LTP}$$

$$[(V_{sat} R_2) / (R_1 + R_2)] + [(V_{ref} R_1) / (R_1 + R_2)] = \text{UTP} \text{----- (1)}$$

$$[(- V_{sat} R_2) / (R_1 + R_2)] + [(V_{ref} R_1) / (R_1 + R_2)] = \text{LTP} \text{----- (2)}$$

Equation (1) – Equation (2)

$$(2 V_{sat} R_2) / (R_1 + R_2) = \text{UTP} - \text{LTP} = 6V$$

Simplifying this equation we get,

$$4 R_2 = R_1$$

Assume R₂ = 1 kΩ R₁ = 10 kΩ

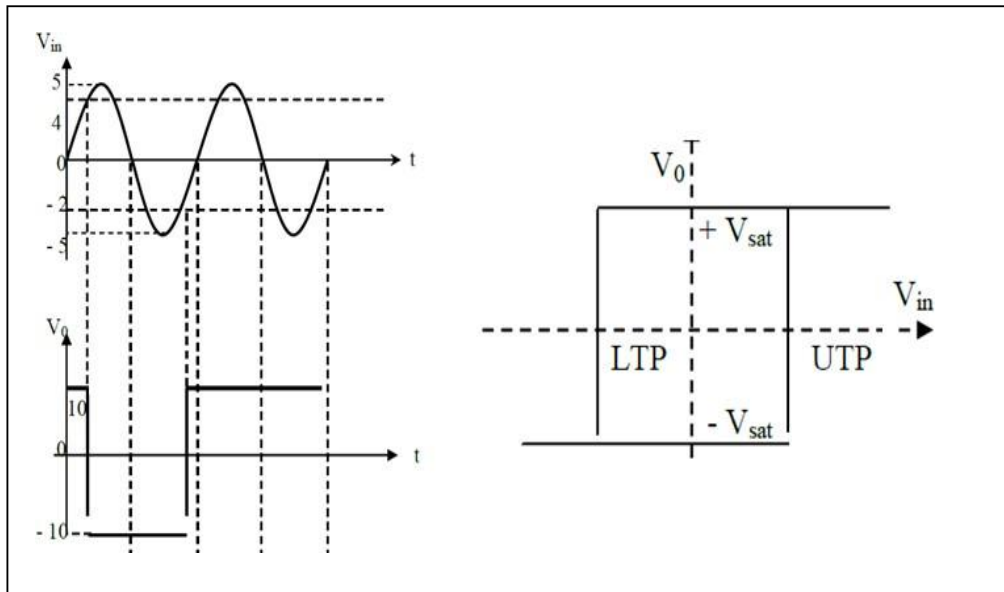
Equation (1) + Equation (2)



$$(2 V_{ref} R_1) / (R_1 + R_2) = UTP + LTP = 2V$$

Simplifying the above equation, we get $V_{ref} = 1.1V$

4.9 Graphs / Outputs



4.10 Results & Analysis

Theoretical Value	UTP =	LTP =
Practical Value	UTP =	LTP =

4.11 Outcome & Conclusion

4.12 Remarks

Faculty Signature



Experiments

5.0 VOLTAGE COMPARATOR AND ZCD

Experiment No	Date Planed	Date Conducted	Marks
05			

5.1 Learning Objectives

1. Study to compare two voltage levels connected at input terminals of op-amp.
2. Design and analyze the zero crossing detector using op-amp.

5.2 Aim

Verify the operation of an op – amp as (a) voltage comparator circuit and (b) Zero Crossing Detector.

5.3 Equipment Required

Sl No	Element	Range	Quantity
5	Op-amp	IC- 741	01
2	Resistor	1 k Ω	02
3	Regulated Power supply	0 – 30V,1A	01
4	Function Generator	1HZ – 1MHz	01
5	Cathode ray oscilloscope	0 – 20MHz	01
6	Bread Board		01

5.4 Theory

- a) **Voltage Comparator:** The circuit diagram shows an op-amp used as a comparator. A fixed reference voltage V_{ref} is applied to the (-) input, and the other time – varying signal voltage V_{in} is applied to the (+) input; Because of this arrangement, the circuit is called the non-inverting comparator. Depending upon the levels of V_{in} and V_{ref} , the circuit produces output. In short, the comparator is a type of analog-to-digital converter. At any given time the output waveform shows whether V_{in} is greater or less than V_{ref} . The comparator is sometimes also called a voltage-level detector because, for a desired value of V_{ref} , the voltage level of the input V_{in} can be detected.
- b) **Zero crossing detector:** ZCD is a **voltage comparator** that switches the output between $+V_{sat}$ and $-V_{sat}$ (V_{sat} : Saturation voltage almost equal to 14V) when the input crosses zero reference voltage. Then **what is a comparator?** In simple words comparators are basic operational amplifier circuits that compare two voltages simultaneously and switches the output according to the comparison. We can say zero crossing detection circuit is a comparator example. We will discuss in detail about comparator in our upcoming articles. Inverting zero cross detector circuit schematic using op amp 741 IC is shown below along with working, input output wave forms.



5.5 Procedure

a) Voltage Comparator

1. A fixed reference voltage V_{ref} is applied to the (-) input, and to the other input a varying voltage V_{in} is applied as shown in Fig 1.
2. Vary the input voltage above and below the V_{ref} and note down the output at pin 6 of IC-741.
3. Observe that,
When V_{in} is less than V_{ref} , the output voltage is $-V_{sat}$ ($\cong -V_{EE}$)
When V_{in} is greater than V_{ref} , the output voltage is $+V_{sat}$ ($\cong +V_{CC}$)

b) Zero crossing detector

1. Connect the circuit as shown in fig 2.
2. Connect supply of 5V peak to peak and 1 kHz at inverting terminal of Op-amp.
3. Observe the waveforms on the CRO. Draw the waveforms on the graph sheet.

5.6 Circuit Diagram

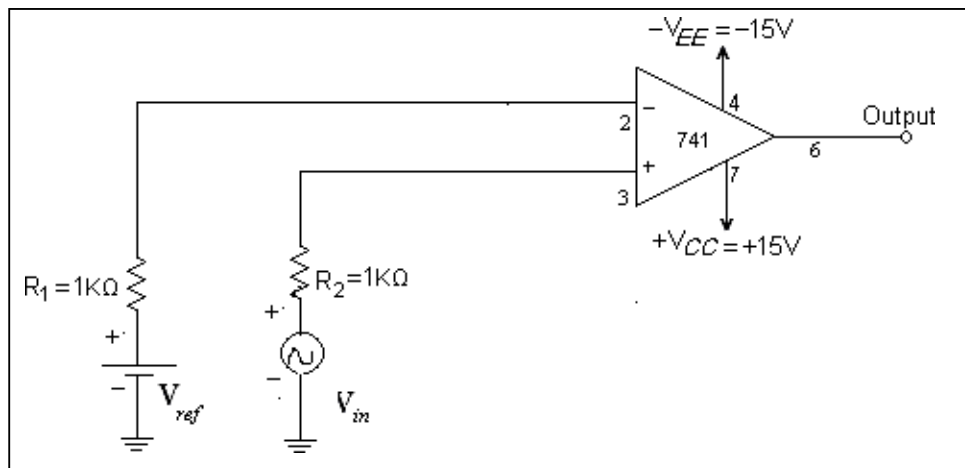


Fig 1 Voltage Comparator Circuit

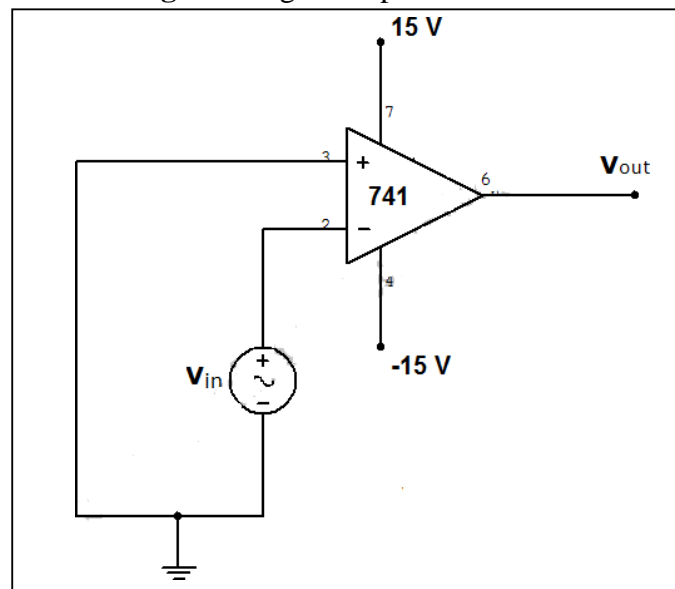


Fig 2 Zero Crossing Detector



5.7 Observation Table

a) Voltage Comparator

Sl No	V_{in}	V_{ref}	V_o
1			
2			
3			

5.8 Formula / Calculations

Comparator

If $V_{in} < V_{ref}$, $V_o = -V_{sat} \cong -V_{EE}$

$V_{in} > V_{ref}$, $V_o = +V_{sat} = +V_{CC}$

5.10 Results & Analysis

5.11 Outcome & Conclusion

5.12 Remarks

Faculty Signature



Experiments

6.0 OP-AMP APPLICATIONS

Experiment No	Date Planed	Date Conducted	Marks
06			

6.1 Learning Objectives

1. Student will be able to design certain op-amp circuits like adder & integrator.
2. Can analyze the op-amp applications.

6.2 Aim

Design and verify the operation of op – amp as an (a) Adder (b) Subtractor (c) Integrator and (d) Differentiator.

6.3 Equipment Required

Sl No	Element	Range	Quantity
1	Op-amp	IC 741	1
2	Resistor	1kΩ 1MΩ 100KΩ	04 01 01
3	Capacitor	0.1μF	1
4	3 Regulated Power supply	0 – 30V, 1A	2
5	Function Generator	0.1–1MHz, 20V _{p-p}	1
6	Cathode Ray Oscilloscope	0 – 20MHz	1
7	Multimeter	--	1
8	Connecting wires	--	Few

6.4 Theory

Adder: A two input summing amplifier may be constructed using the inverting mode. The adder can be obtained by using either non-inverting mode or differential amplifier. Here the inverting mode is used. So the inputs are applied through resistors to the inverting terminal and non-inverting terminal is grounded. This is called “virtual ground”, i.e. the voltage at that terminal is zero. The gain of this summing amplifier is 1, any scale factor can be used for the inputs by selecting proper external resistors.

Subtractor: A basic differential amplifier can be used as a subtractor as shown in the circuit diagram. In this circuit, input signals can be scaled to the desired values by selecting appropriate values for the resistors. When this is done, the circuit is referred to as scaling amplifier. However in this circuit all external resistors are equal in value. So the gain of amplifier is equal to one. The output voltage V_o is equal to the voltage applied to the non-inverting terminal minus the voltage applied to the inverting terminal; hence the circuit is called a subtractor.

Integrator: In an integrator circuit, the output voltage is integral of the input signal. The output voltage of an integrator is given by $V_o = -1/R_1 C_f \int_0^t V_{i(p-p)} dt$
At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor.



Differentiator: In the differentiator circuit the output voltage is the differentiation of the input voltage. The output voltage of a differentiator is given by $V_o = -R_f C_1 (dV_i/dt)$. The input impedance of this circuit decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. At high frequencies circuit may become unstable.

6.5 Procedure

A) For Adder:

1. Connect the circuit as per the diagram shown in Fig 1.
2. Apply the supply voltages of +15V to pin 7 and pin 4 of IC741 respectively.
3. Apply the inputs V_1 and V_2 as shown in Fig 1.
4. Apply two different signals (DC/AC) to the inputs.
5. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741.
6. Notice that the output is equal to the sum of the two inputs.

B) For Subtractor:

1. Connect the circuit as per the diagram shown in Fig 2.
2. Apply the supply voltages of +15V to pin7 and pin4 of IC741 respectively.
3. Apply the inputs V_1 and V_2 as shown in Fig 2.
4. Apply two different signals (DC/AC) to the inputs
5. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741.
6. Notice that the output is equal to the difference of the two inputs.

C) For Integrator

1. Connect the circuit as per the diagram shown in Fig 3
2. Apply a square wave/sine input of 4V (p-p) at 1 KHz.
3. Observe the output at pin 6.
4. Draw input and output waveforms.

D) For Differentiator

1. Connect the circuit as per the diagram shown in Fig 4
2. Apply a square wave/sine input of 4V (p-p) at 1 KHz.
3. Observe the output at pin 6.
4. Draw the input and output waveforms.

6.6 Circuit Diagram

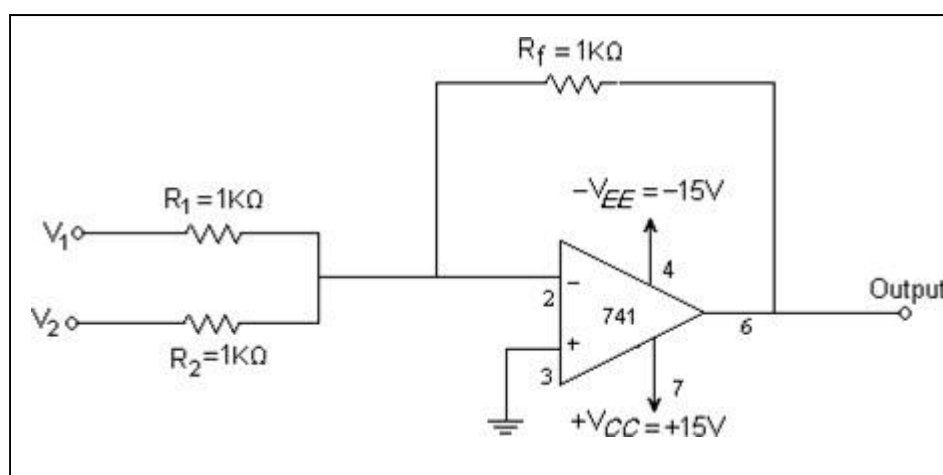


Fig 1 Adder Circuit

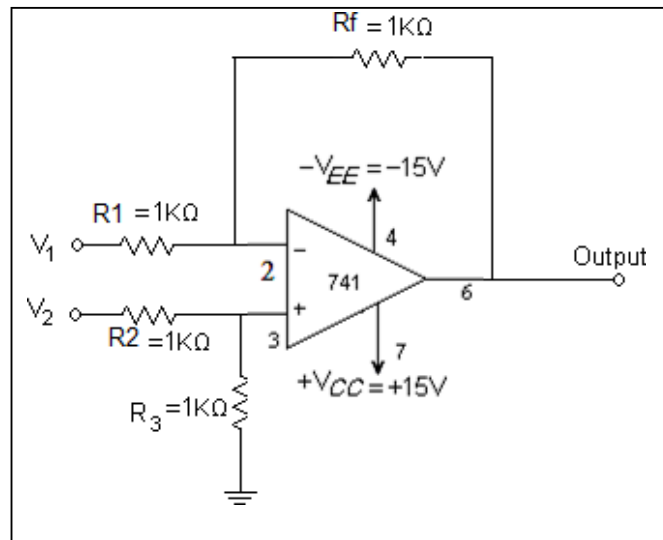


Fig 2 Subtractor Circuit

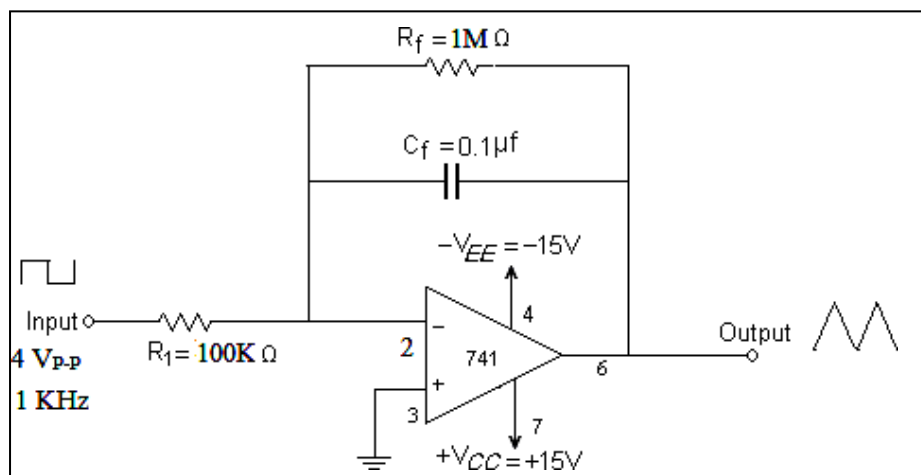


Fig 3 Integrator Circuit

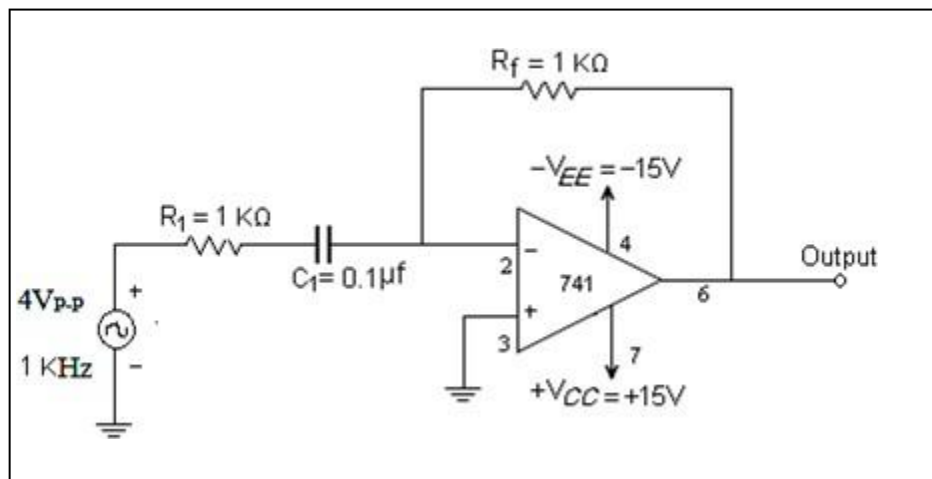


Fig 4 Differentiator Circuit



6.7 Observation Table

a) Adder

V ₁ (Volts)	V ₂ (Volts)	V ₀ (Volts)

b) Subtractor

V ₁ (Volts)	V ₂ (Volts)	V ₀ (Volts)

c) Integrator

Input- Square Wave		Output- Spikes	
Amplitude (p-p) V	Time Period mS	Amplitude (p-p) V	Time Period mS

Input- Sine Wave		Output- Cosine Wave	
Amplitude (p-p) V	Time Period mS	Amplitude (p-p) V	Time Period mS

d) Differentiator

Input- Square Wave		Output- Triangular Wave	
Amplitude (p-p) V	Time Period mS	Amplitude (p-p) V	Time Period mS

Input- Sine Wave		Output- Cosine Wave	
Amplitude (p-p) V	Time Period mS	Amplitude (p-p) V	Time Period mS

6.8 Formula / Calculations

Design Equations

c) Integrator:

Choose $T = 2\pi R_f C_f$

Where T= Time period of the input signal

Assume C_f and find R_f

Select $R_f = 10R_1$

$$V_o = -1/R_1 C_f \int_0^t V_{i(p-p)} dt$$



d) Differentiator:

Select given frequency $f_a = 1/(2\pi R_f C_1)$, Assume C_1 and find R_f

Select $f_b = 10 f_a = 1/2\pi R_1 C_1$ and find R_1

From $R_1 C_1 = R_f C_f$, find C_f

Calculations

a) Adder

$$V_0 = - (V_1 + V_2)$$

If $V_1 = 2.5V$ and $V_2 = 2.5V$, then

$$V_0 = - (2.5+2.5) = -5V.$$

c) Integrator:

For $T = 1$ msec

$$f_a = 1/T = 1 \text{ KHz}$$

$$f_a = 1 \text{ KHz} = 1/(2\pi R_f C_f)$$

Assuming

$$C_f = 0.1 \mu\text{f}, R_f \text{ is found from } R_f = 1/(2\pi f_a C_f)$$

$$R_f = 1.59 \text{ K}\Omega$$

$$R_f = 10 R_1$$

$$R_1 = 159 \Omega$$

b) Subtractor

$$V_0 = V_2 - V_1$$

If $V_1 = 2.5$ and $V_2 = 3.3$, then

$$V_0 = 3.3 - 2.5 = 0.8V$$

d) Differentiator

For $T = 1$ msec

$$f = 1/T = 1 \text{ KHz}$$

$$f_a = 1 \text{ KHz} = 1/(2\pi R_f C_1)$$

Assuming

$$C_1 = 0.1 \mu\text{f}, R_f \text{ is found from } R_f = 1/(2\pi f_a C_1)$$

$$R_f = 1.59 \text{ K}\Omega$$

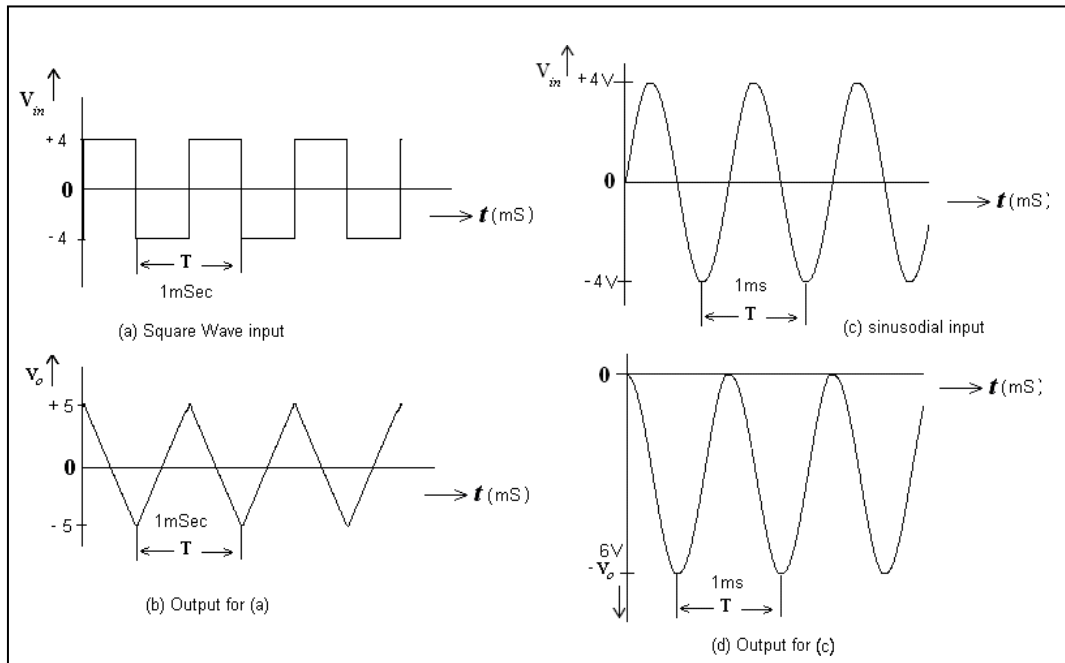
$$f_b = 10 f_a = 1/2\pi R_1 C_1$$

for $C_1 = 0.1 \mu\text{f}$;

$$R_1 = 159 \Omega$$

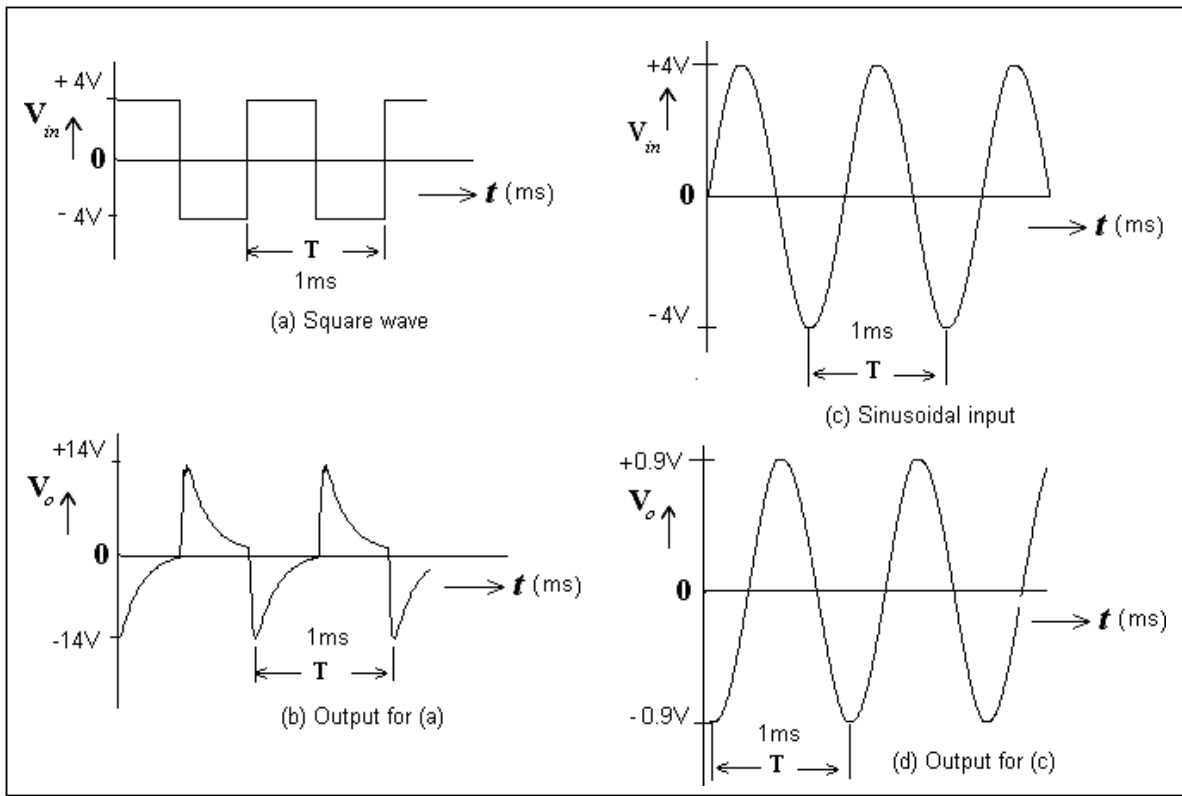
6.9

Outputs





Differentiator



6.10 Results & Analysis

6.11 Outcome & Conclusion

6.12 Remarks

Faculty Signature



Experiments

7.0 ACTIVE FILTERS

Experiment No	Date Planed	Date Conducted	Marks
07			

7.1 Learning Objectives

1. Designing and verifying the op-amp acting as filters.
2. Different types of filters are designed by minute changes in the circuit.

7.2 Aim

Design and realize an op – amp based first order Butterworth (a) low pass (b) high pass and (c) band pass filters for a given cut off frequency/frequencies to verify the frequency response characteristic.

7.3 Equipment Required

Sl No	Element	Range	Quantity
1	Op-amp	IC- 741	01
2	Resistors	10 K Ω 1.5K Ω 15K Ω	03 01 01
3	Capacitor	0.01 μ f 100nF 3.3nF	01 01 01
4	CRO	0 – 20MHz	01
5	Regulated Power supply	0 – 30V,1A	01
6	Function Generator	1Hz – 1MHz	01

7.4 Theory

a) LPF:

A LPF allows frequencies from 0 to higher cut of frequency, f_H . At f_H the gain is 0.707 A_{max} , and after f_H gain decreases at a constant rate with an increase in frequency. The gain decreases 20dB each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_H is 20dB/decade or 6 dB/ octave, where octave signifies a two fold increase in frequency. The frequency $f=f_H$ is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB from 0 Hz. Other equivalent terms for cut-off frequency are -3dB frequency, break frequency, or corner frequency.

b) HPF:

The frequency at which the magnitude of the gain is 0.707 times the maximum value of gain is called low cut off frequency. Obviously, all frequencies higher than f_L are pass band frequencies with the highest frequency determined by the closed –loop band width all of the op-amp



c) BPF:

A band-pass filter is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range.

A band pass signal is a signal containing a band of frequencies not adjacent to zero frequency, such as a signal that comes out of a band pass filter.

A pass band is the range of frequencies or wavelengths that can pass through a filter. A band pass-filtered signal (that is, a signal with energy only in a pass band), is known as a band pass signal contrary to a baseband signal.

7.5 Procedure

First Order LPF

1. Connections are made as per the circuit diagram shown in Fig 1.
2. Apply sinusoidal wave of constant amplitude as input.
3. Vary the input frequency and note down the output amplitude at each step.
4. Plot the frequency response as shown in Fig 4.

First Order HPF:

1. Connections are made as per the circuit diagrams shown in Fig 2.
2. Apply sinusoidal wave of constant amplitude as input.
3. Vary the input frequency and note down the output amplitude at each step.
4. Plot the frequency response as shown in Fig 5.

First Order BPF:

1. Connections are made as per the circuit diagrams shown in Fig 3.
2. Apply sinusoidal wave of constant amplitude as input.
3. Vary the input frequency and note down the output amplitude at each step.
4. Observe the output at lower and upper cut off frequency points.
5. Plot the frequency response as shown in Fig 6.

7.6 Circuit Diagram

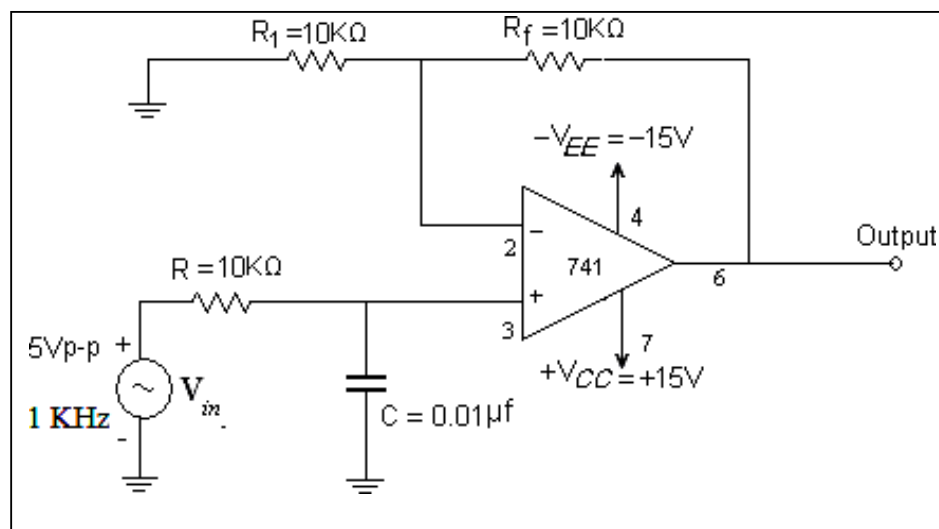


Fig 1 First Order Low Pass Filter Circuit

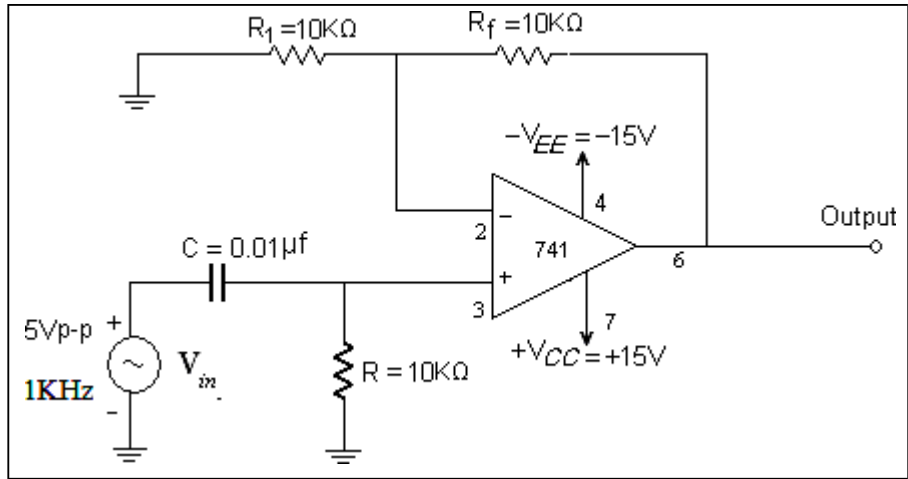


Fig 2 First Order High Pass Filter Circuit

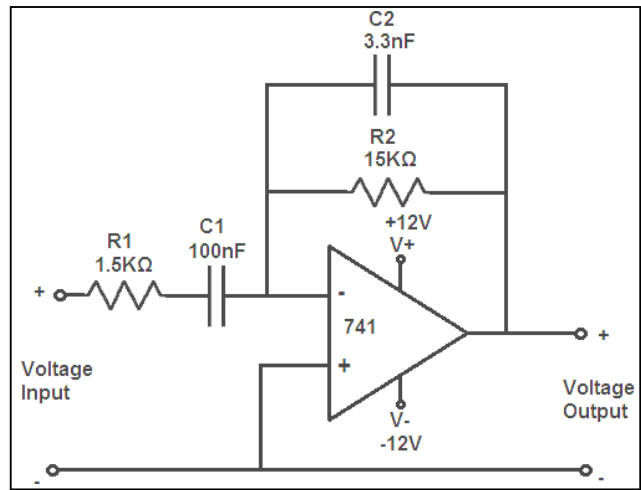


Fig 3 First Order Band Pass Filter Circuit

7.7 Observation Table

Input Voltage = 0.5V

a) LPF

Sl No	Frequency	Output Voltage (V)	Voltage Gain V_o/V_i	Gain In dB

b)HPF

Sl No	Frequency	Output Voltage (V)	Voltage Gain V_o/V_i	Gain In dB



c) BPF

Sl No	Frequency	Output Voltage (V)	Voltage Gain V_o/V_i	Gain In dB

7.8 Formula / Calculations

First Order LPF:

To design a Low Pass Filter for higher cut off frequency $f_H = 4$ KHz and pass band gain of 2.

$$f_H = 1 / (2\pi RC)$$

Assuming $C=0.01 \mu F$, the value of R is found from

$$R = 1 / (2\pi f_H C) \Omega = 3.97 K\Omega$$

The pass band gain of LPF is given by $A_F = 1 + (R_F/R_1) = 2$

Assuming $R_1=10 K\Omega$, the value of R_F is found from

$$R_F = (A_F - 1) R_1 = 10 K\Omega$$

First Order HPF:

To design a High Pass Filter for lower cut off frequency $f_L = 4$ KHz and pass band gain of 2

$$f_L = 1 / (2\pi RC)$$

Assuming $C=0.01 \mu F$, the value of R is found from

$$R = 1 / (2\pi f_L C) \Omega = 3.97 K\Omega$$

The pass band gain of HPF is given by $A_F = 1 + (R_F/R_1) = 2$

Assuming $R_1=10 K\Omega$, the value of R_F is found from

$$R_F = (A_F - 1) R_1 = 10 K\Omega$$



7.9 Graphs

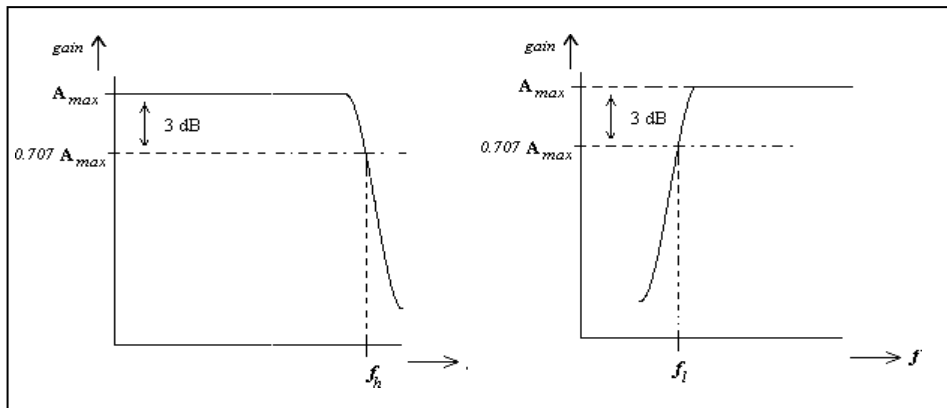


Fig 4 Frequency Response of LPF

Fig 5 Frequency Response of HPF

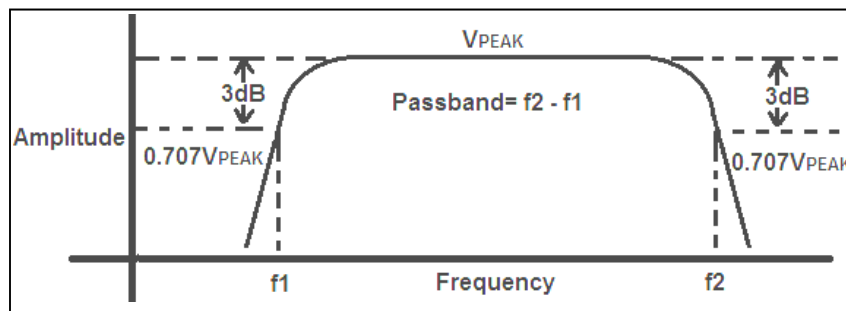


Fig 6 Frequency Response of BPF

7.10 Results & Analysis

7.11 Outcome & Conclusion

7.12 Remarks

Faculty Signature



Experiments

8.0 FUNCTION GENERATOR

Experiment No	Date Planed	Date Conducted	Marks
08			

8.1 Learning Objectives

1. Student will study the generation of different waves using op-amp.
2. Usage of op-amp in wave shaping circuits.

8.2 Aim

Design and realize an op – amp based function generator to generate sine, square and triangular waves of desired frequency.

8.3 Equipment Required

Sl No	Element	Range	Quantity
1	Op-amp	741 IC	02
2	Capacitors	0.01 μ f,0.001 μ f 0.05 μ f	01 each 02
3	Resistors	86k Ω ,68k Ω ,680k Ω 100k Ω , 3.3k Ω 12 k Ω	01 each 02 each 01
4	Potentiometer	50k Ω	01
5	Regulated Power supply	0-30 V 1A	01
6	Cathode Ray Oscilloscope	0 -20MHz	01

8.4 Theory

Function generator generates waveforms such as sine, triangular, square waves and so on of different frequencies and amplitudes. The circuit shown in Fig1 is a simple circuit which generates square waves and triangular waves simultaneously. Here the first section is a square wave generator and second section is an integrator. When square wave is given as input to integrator it produces triangular wave.

8.5 Procedure

1. Connect the circuit as per the circuit diagram shown above.
2. Obtain square wave at terminal A and Triangular wave at V_{o2} as shown in Fig 1 and sine wave output at V_o of Fig 2.
3. Adjust Potentiometer to get the sine wave.
4. Draw the output waveforms.



8.6 Circuit Diagram

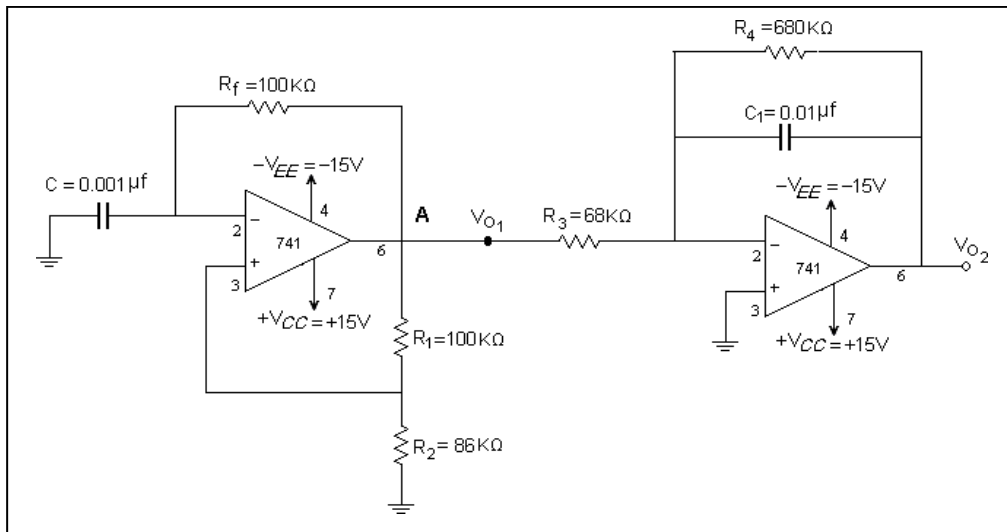


Fig 1 Function Generator Circuit

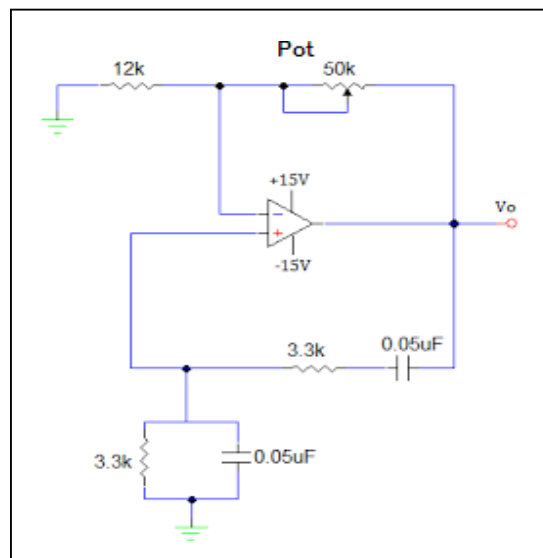


Fig 2 Sine Wave Generator Circuit

8.7 Observation Table

	Peak to Peak Voltage V_{p-p}	Time Period T
Square Wave:		
Triangular Wave:		
Sine Wave:		

8.8 Formula / Calculations

Square wave Generator:

$$T = 2R_f C \ln(2R_2 + R_1 / R_1)$$

Assume $R_1 = 1.16 R_2$

Then $T = 2R_f C$

Assume C and find R_f

Assume R_1 and find R_2

Integrator:

Take $R_3 C_f \gg T$

$$R_3 C_f = 10T$$

Assume C_f find R_3

Take $R_3 C_f = 10T$

Assume $C_f = 0.01 \mu f$

$$R_3 = 10T / C = 20K\Omega$$



For $T = 2 \text{ msec}$

$$T = 2R_f C$$

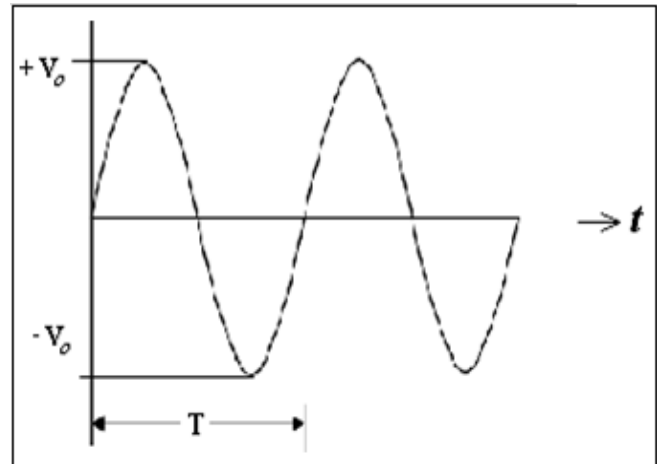
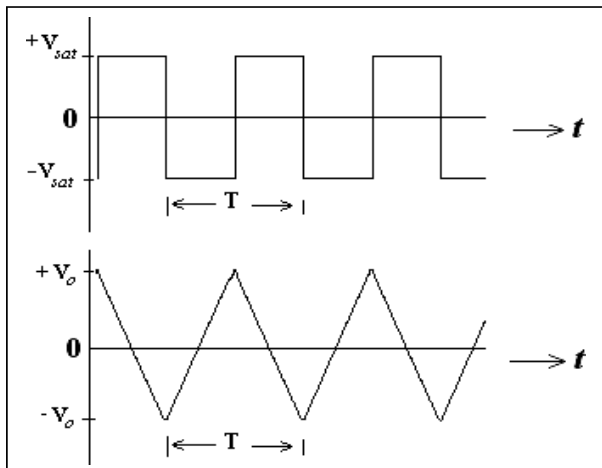
Assuming $C = 0.1 \mu\text{f}$

$$R_f = \frac{2 \times 10^{-3}}{2 \times 0.1 \times 10^{-6}} \\ = 10 \text{ K}\Omega$$

Assuming $R_1 = 100 \text{ K}$

$$R_2 = 86 \text{ K}\Omega$$

8.9 Graphs / Outputs



8.10 Results & Analysis

8.11 Outcome & Conclusion

8.12 Remarks

Faculty Signature



Experiments

9.0 R – 2R LADDER DAC.

Experiment No	Date Planed	Date Conducted	Marks
09			

9.1 Learning Objectives

Student aims to convert digital value to analog signal

9.2 Aim

Design and realization of R – 2R ladder DAC.

9.3 Equipment Required

Sl No	Elements	Range	Quantity
1	Op-amp	IC-741	01
2	Resistors	1K Ω 2K Ω	03 07
3	Regulated power supply	0-30 V, 1A	01
4	Multimeter	--	01
5	Digital Trainer Board	--	01
6	Connecting wires	--	Few

9.4 Theory

Nowadays digital systems are used in many applications because of their increasingly efficient, reliable and economical operation. Since digital systems such as microcomputers use a binary system of ones and zeros, the data to be put into the microcomputer have to be converted from analog form to digital form. The circuits that perform this conversion and reverse conversion are called A/D and D/A converters respectively. D/A converter in its simplest form use an op-amp and resistors either in the binary weighted form or R-2R form. The fig. below shows D/A converter with resistors connected in R-2R form. It is so called as the resistors used here are R and 2R. The binary inputs are simulated by switches b₀ to b₃ and the output is proportional to the binary inputs. Binary inputs are either in high (+5V) or low (0V) state. The analysis can be carried out with the help of Thevenin's theorem. The output voltage corresponding to all possible combinations of binary inputs can be calculated as below.

$$V_0 = -R_f [(b_3 V_R/2R) + (b_2 V_R/4R) + (b_1 V_R/8R) + (b_0 V_R/16R)]$$

Where each inputs b₃, b₂, b₁ and b₀ may be high (+5V) or low (0V).

The great advantage of D/A converter of R-2R type is that it requires only two sets of precision resistance values. In weighted resistor type more resistors are required and the circuit is complex. As the number of binary inputs is increased beyond 4 even D/A converter circuits get complex and their accuracy degenerates. Therefore in critical applications IC D/A converter is used. Some of the parameters must be known with reference to converters, resolution, linearity error, settling time etc.

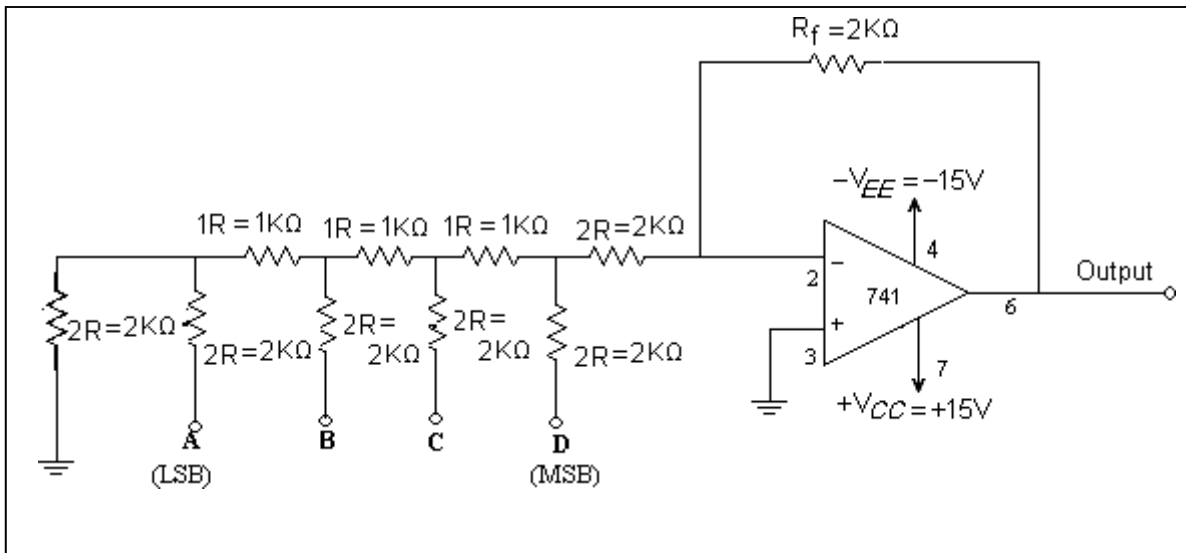
$$\text{Resolution} = 0.5V / 28 = 5 / 256 = 0.0195$$



9.5 Procedure

1. Connect the circuit as shown in Fig 1.
2. Vary the inputs A, B, C, D from the digital trainer board and note down the output at pin 6. For logic „1“, 5 V is applied and for logic „0“, 0 V is applied.
3. Repeat the steps for different values

9.6 Circuit Diagram



1.7 Observation Table

SI No	D (MSB)	C	B	A (LSB)	Theoretical Voltage (V)	Practical Voltage (V)
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						

9.8 Formula / Calculations

The equation for output voltage is given by

$$V_0 = - R_f [(b_3 V_R / 2R) + (b_2 V_R / 4R) + (b_1 V_R / 8R) + (b_0 V_R / 16R)]$$

$$V_0 = - R_f \cdot V_R [(b_3 / 2R) + (b_2 / 4R) + (b_1 / 8R) + (b_0 / 16R)]$$

Case (i) If $b_0 b_1 b_2 b_3 = 1 0 0 0$ for 0.5 volts change in output for LSB change

$$- 0.5 = - 20 \times 10^3 \cdot V_{ref} [(1 / (16 \times 1.10^3)) + 0 + 0 + 0]$$



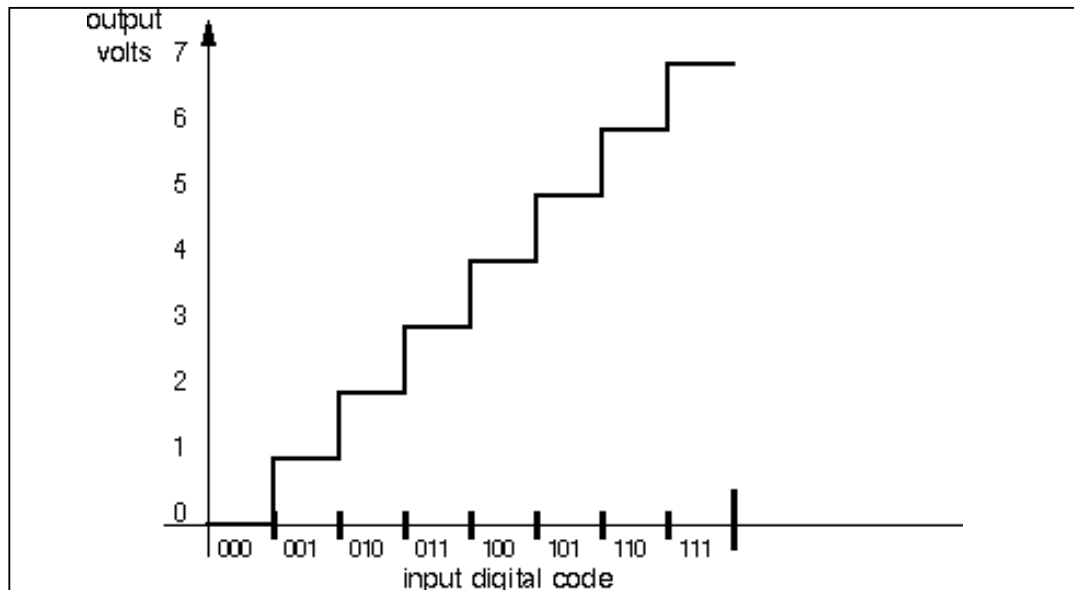
$V_{ref} = 4V$

Case (ii) If $V_{ref} = 5V$ and $b_0 b_1 b_2 b_3 = 0 1 0 0$, then

$$V_0 = -20.103 \cdot 5 \left[(0 + (1/8.1.103)) + 0 + 0 \right]$$

$$V_0 = -1.25V$$

9.9 Graphs



9.10 Results & Analysis

9.11 Outcome & Conclusion

9.12 Remarks

Faculty Signature



Experiments

11.0 PULSE GENERATOR USING 555

Experiment No	Date Planed	Date Conducted	Marks
11			

11.1 Learning Objectives

Student study one of the operating mode of 555 timer that is monostable multivibrator mode.

11.2 Aim

Design and verify an IC 555 timer based pulse generator for the specified pulse.

11.3 Equipment Required

SI No	Element	Range	Quantity
1	555-Timer	IC- 555	01
2	Capacitors	0.1 μ f, 0.01 μ f	Each one
3	Resistor	10k Ω	01
4	Regulated Power supply	0 – 30V,1A	01
5	Function Generator	1HZ – 1MHz	01
6	Cathode ray oscilloscope	0 – 20MHz	01

11.4 Theory

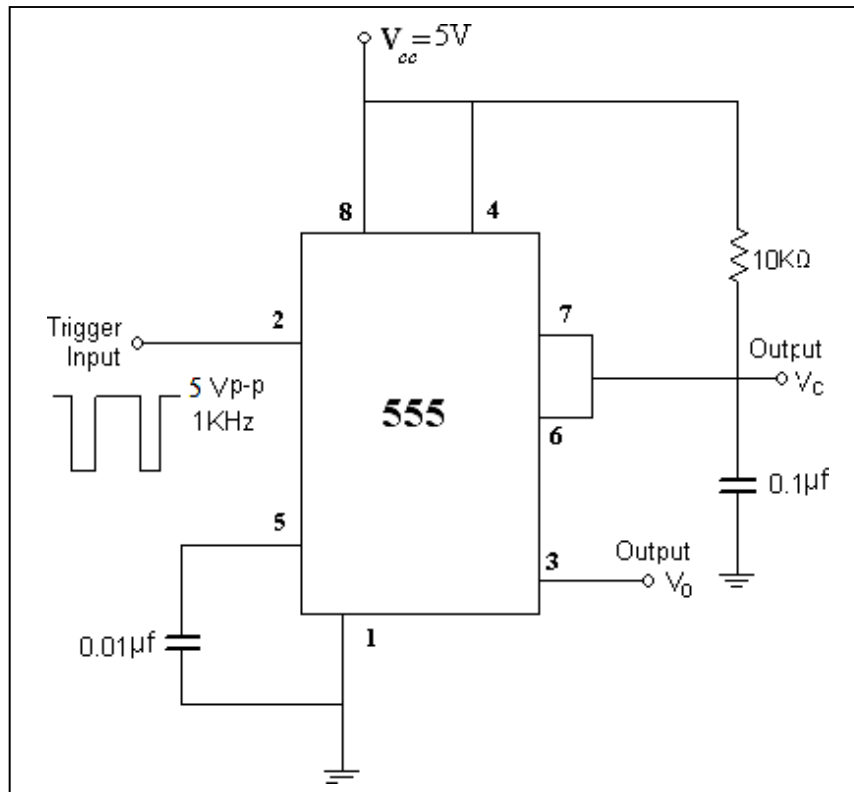
A Monostable Multivibrator, often called a one-shot Multivibrator, is a pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby mode the output of the circuit is approximately Zero or at logic low level. When an external trigger pulse is obtained, the output is forced to go high (approx V_{CC}). The time for which the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The Monostable circuit has only one stable state (output low), hence the name monostable. Normally the output of the Monostable Multivibrator is low.

11.5 Procedure

1. Connect the circuit as shown in the circuit diagram.
2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz.
3. Observe the output waveform and measure the pulse duration.
4. Theoretically calculate the pulse duration as $T_{ON}=1.1. R_A C$
5. Compare it with experimental values.



11.6 Circuit Diagram



11.7 Observation Table

Sl no	R	C	Theoretical $T_p = 1.1 RC$	Practical T_p

11.8 Formula / Calculations

DESIGN:

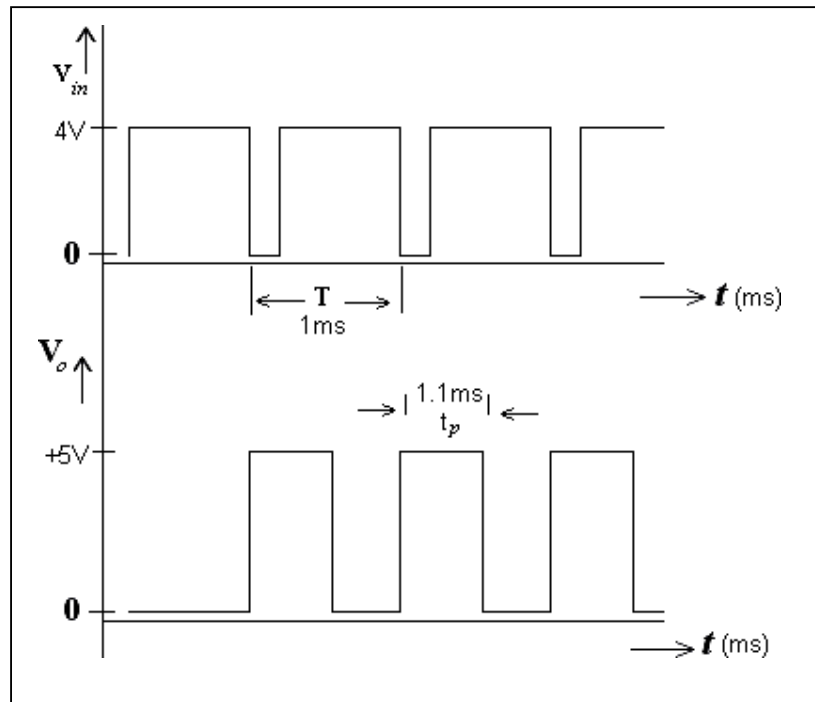
Consider $V_{CC} = 5V$, for given t_p
Output pulse width $t_p = 1.1 R_A C$
Assume C in the order of microfarads & Find R_A

Typical values:

If $C = 0.1 \mu F$, $R_A = 10k$ then $t_p = 1.1 \text{ mSec}$
Trigger Voltage = 4 V



11.9 Outputs



11.10 Results & Analysis

11.11 Outcome & Conclusion

11.12 Remarks

Faculty Signature



Experiments

12.0 VOLTAGE REGULATOR

Experiment No	Date Planed	Date Conducted	Marks
12			

12.1 Learning Objectives

Student study both positive voltage regulation as well as negative voltage regulation using IC 78** and 79** series.

12.2 Aim

Designing of Fixed voltage power supply (voltage regulator) using IC regulators 78 & 79 series.

12.3 Equipment Required

Sl No	Element	Range	Quantity
1	Bread board		01
2	IC7805		01
3	IC7809		01
4	IC7912		01
5	Multimeter		01
6	Milli ammeter	0-150 mA	01
7	Regulated power supply	0-30 V 1A	01
8	Resistors pot	100Ω ,1k Ω	01

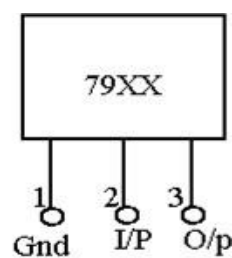
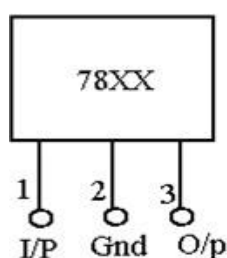
12.4 Theory

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage. IC voltage regulators are versatile, relatively inexpensive and are available with features such as programmable output, current/voltage boosting, internal short circuit current limiting, thermal shunt down and floating operation for high voltage applications.

The 78XX series consists of three-terminal positive voltage regulators with seven voltage options. These IC's are designed as fixed voltage regulators and with adequate heat sinking can deliver output currents in excess of 1A.

The 79XX series of fixed output voltage regulators are complements to the 78XX series devices. These negative regulators are available in same seven voltage options. Typical performance parameters for voltage regulators are line regulation, load regulation, temperature stability and ripple rejection.

Pin Configurations:





12.5 Procedure

a) Line Regulation:

1. Connect the circuit as shown in Fig 1 by keeping S open for 7805.
2. Vary the dc input voltage from 0 to 10V in suitable stages and note down the output voltage in each case, and plot the graph between input voltage and output voltage.
3. Repeat the above steps for negative voltage regulator as shown in Fig.2 for 7912 for an input of 0 to -15V.
4. Note down the dropout voltage whose typical value = 2V and line regulation typical value = 4mv for $V_{in} = 7V$ to 25V.

b) Load regulation:

1. Connect the circuit as shown in the Fig 1 by keeping S closed for load regulation.
2. Now vary R_L and measure current I_L and note down the output voltage V_o in each case and plot the graph between current I_L and V_o .
3. Repeat the above steps as shown in Fig 2 by keeping switch S closed for negative voltage regulator 7912.

12.6 Circuit Diagram

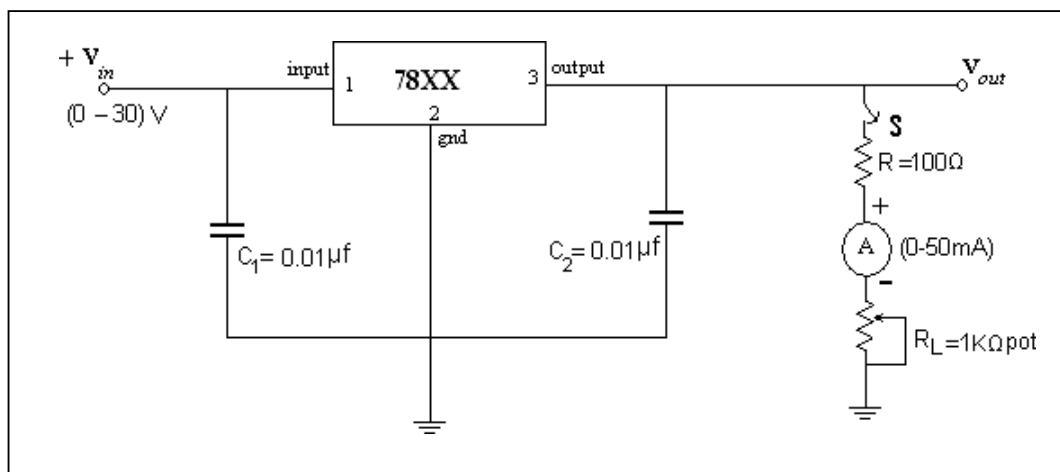


Fig 1 Positive Voltage Regulator Circuit

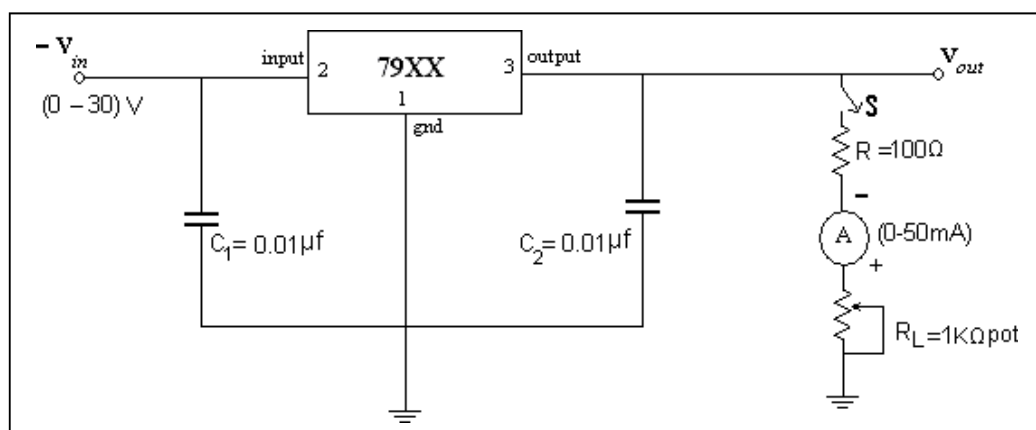


Fig 2 Negative Voltage Regulator Circuit



12.7 Observation Table

IC- 7805

Line Regulation

Load Regulation $V_{NL} = 15\text{ V}$

Vi (V)	Vo (V)

Load Current (mA)	Load Resistance RL(Ω)	Vdc (FL) (V)	% Regulation

IC- 7912

Line Regulation

Load Regulation V_{NL}

Vi (V)	Vo (V)

Load Current (mA)	Load Resistance RL(Ω)	Vdc(FL) (V)	% Regulation

12.8 Formula / Calculations

Output Resistance:

$$R_o = \frac{(V_{NL} - V_{FL})}{I_{FL}} \Omega$$

V_{NL} - load voltage with no load current

V_{FL} - load voltage with full load current

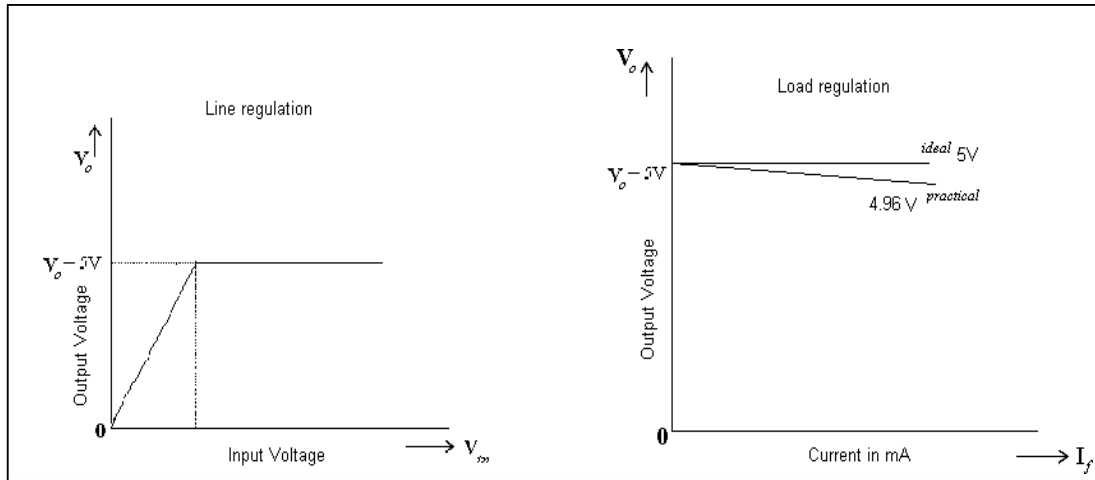
I_{FL} - full load current

$$\% \text{ load regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

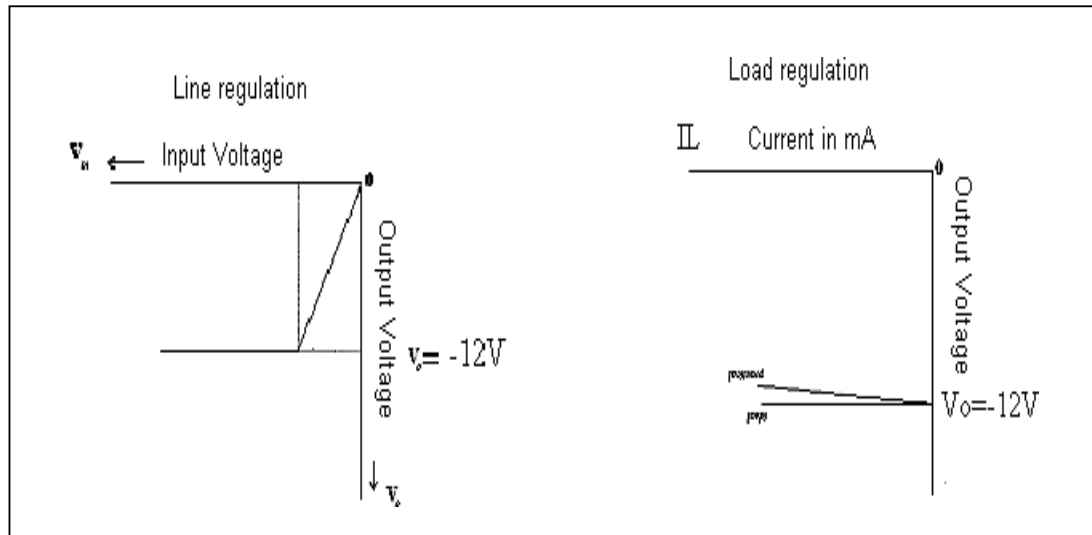


12.9 Graphs / Outputs

IC 7805



IC- 7912



12.10 Results & Analysis

12.11 Outcome & Conclusion

12.12 Remarks

Faculty Signature