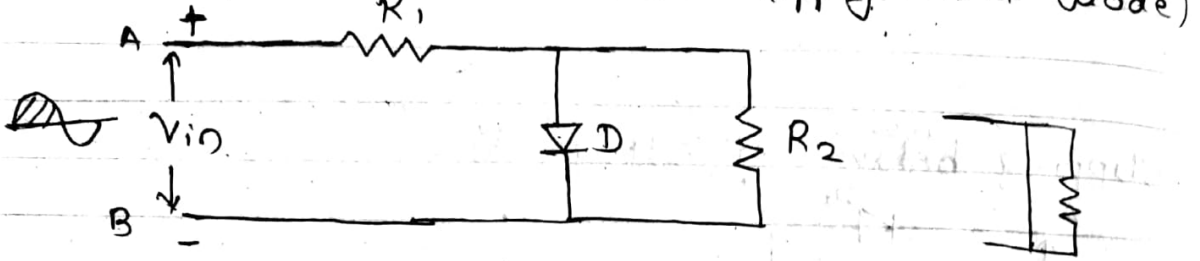
*Clipper:- The ckt. which remove certain part of the waveform.

★ Parallel Clipper:-

★ Basic ||el clipper with +ve clipping (ideal diode)



+ve half cycle

$i_2 = 0$ Diode = F.B

$V_o = 0V$

-ve half cycle

Diode = R.B

$\therefore i_2 = i_2$

$V_o = V_{in} \frac{R_L}{R_1 + R_L}$ $R_L >> R_1$

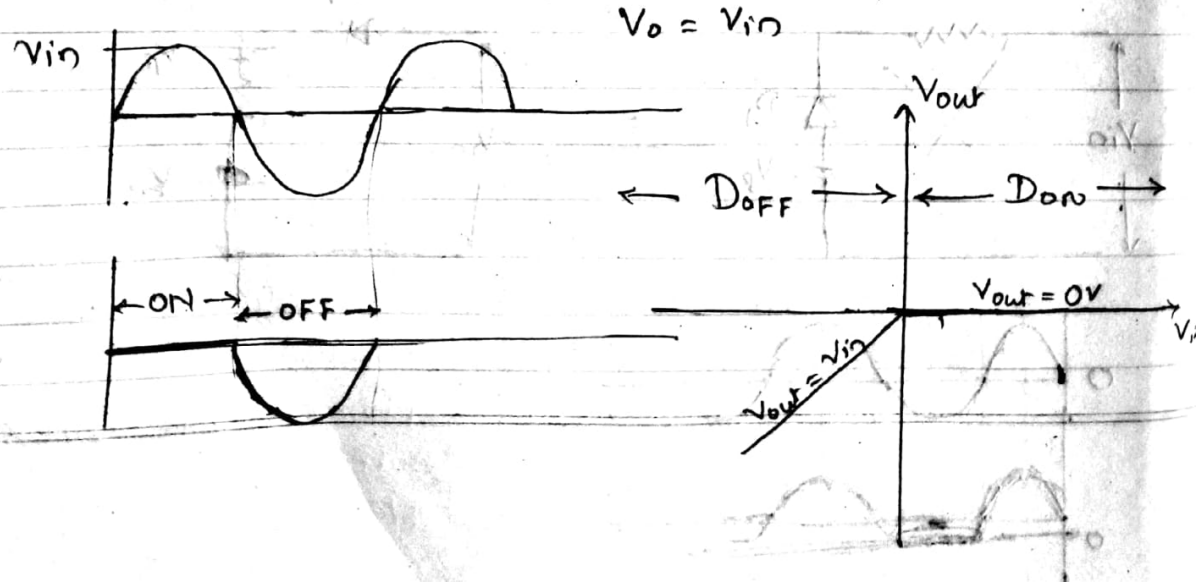
$V_o \propto V_{in}$

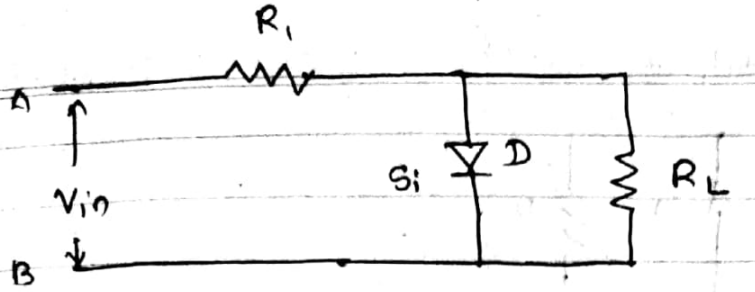
For $V_{in} > 0$ $V_o = 0V$

$V_{in} < 0$ $V_o = V_{in} \frac{R_L}{R_1 + R_L}$

AS $R_L >> R_1$

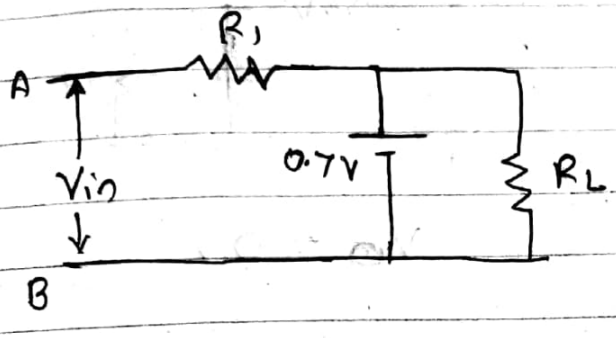
$V_o = V_{in}$





+ve half cycle

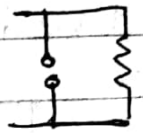
Diode is ⇒ 

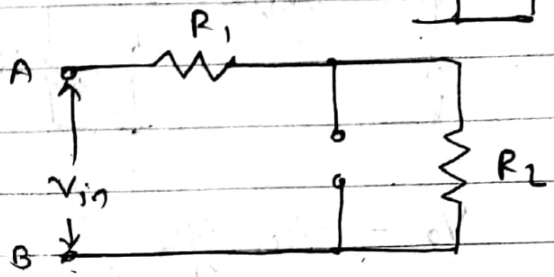


$V_{in} > 0$

$V_o = 0.7\,V$

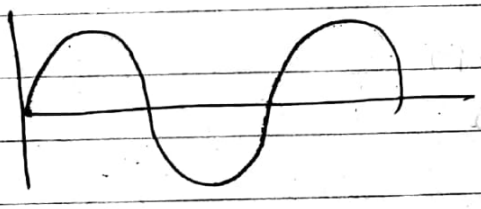
-ve half cycle

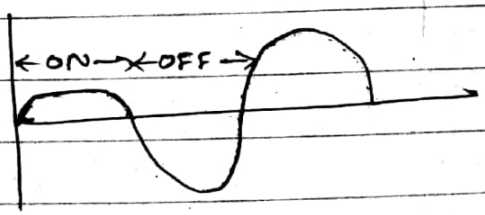
Diode is 

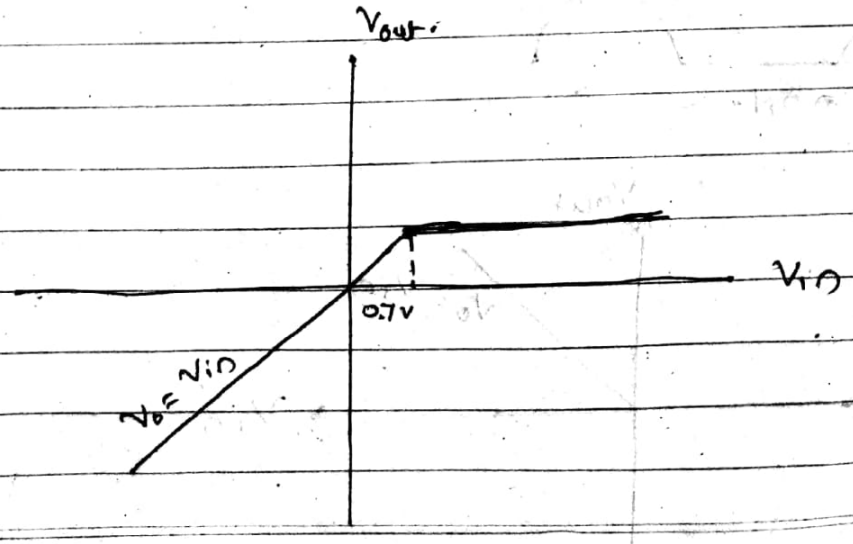


$V_{in} < 0$

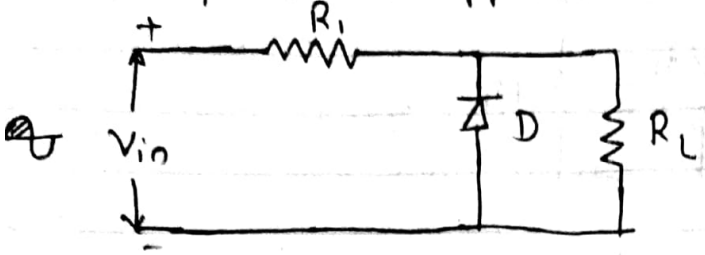
$V_o = V_{in}$



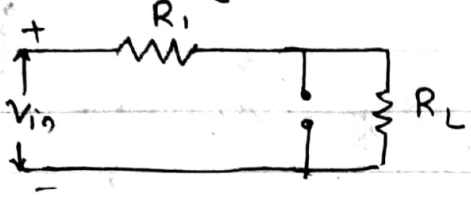




★ Basic parallel clipper with negative clipping



+ve half cycle

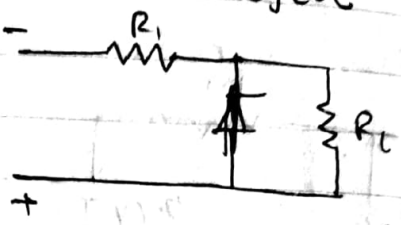


$$V_o = V_{in} \frac{R_L}{R_1 + R_L}$$

$R_L >> R_1$

$V_o = V_{in}$

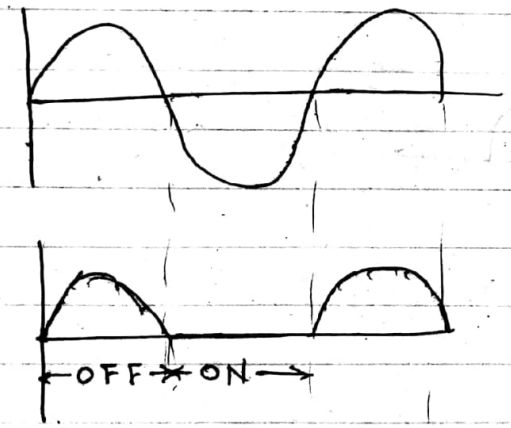
-ve half cycle

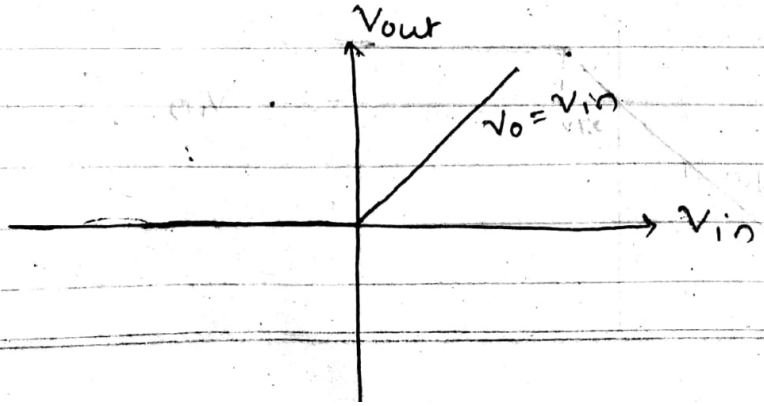


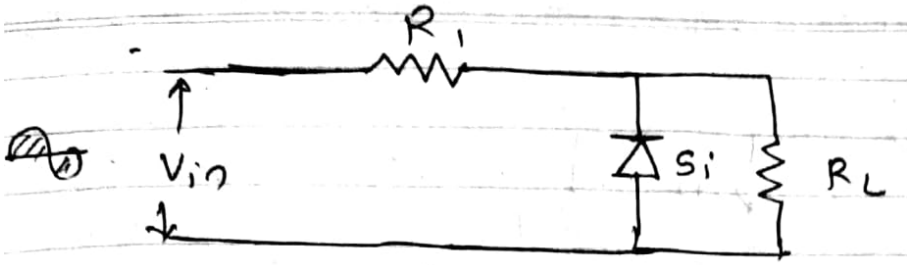
$V_o = 0\ V$

$V_{in} > 0$ $\quad V_o = V_{in}$

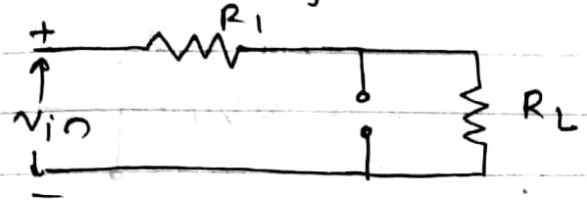
$V_{in} < 0$ $\quad V_o = 0$







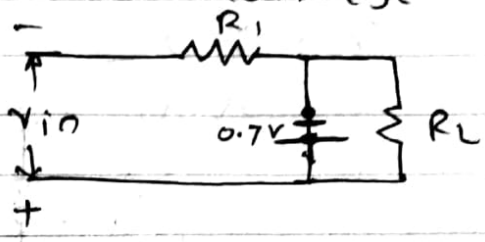
+ve half cycle



$$V_o = V_{in} \frac{R_L}{R_1 + R_L}$$

$$V_o \simeq V_{in}$$

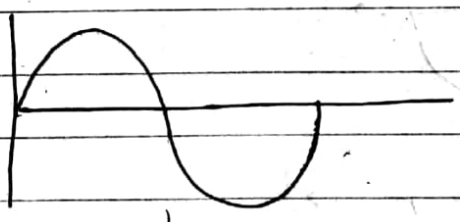
-ve half cycle

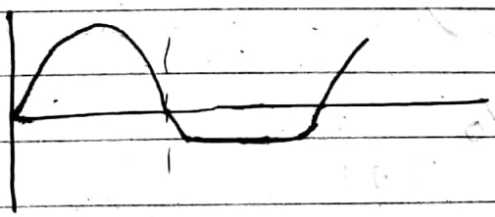


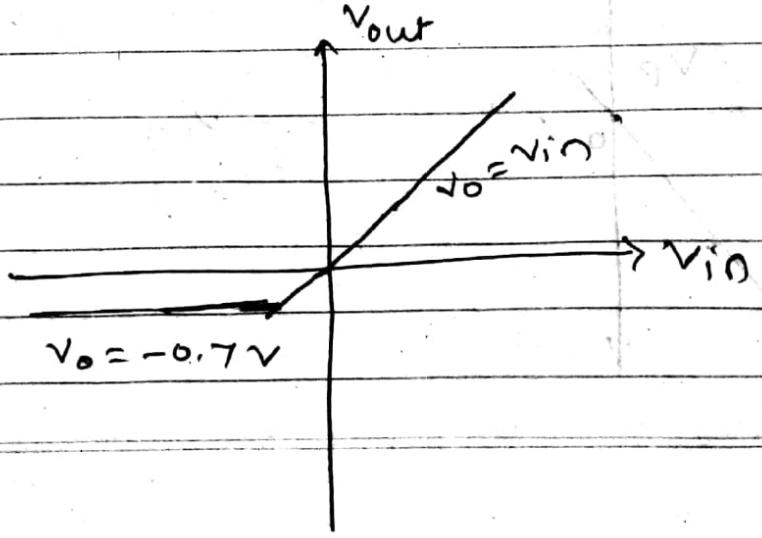
$V_o = -0.7\ V$

$V_{in} > 0 \qquad V_o \simeq V_{in}$

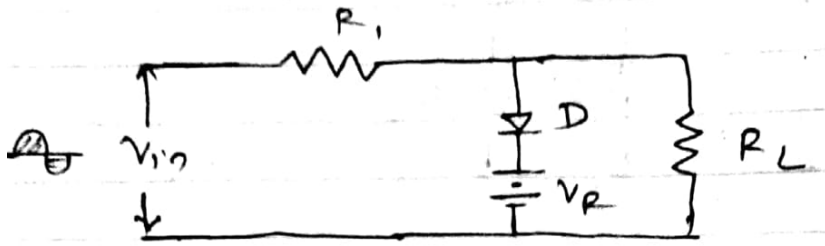
$V_{in} < 0 \qquad V_o = -0.7\ V$



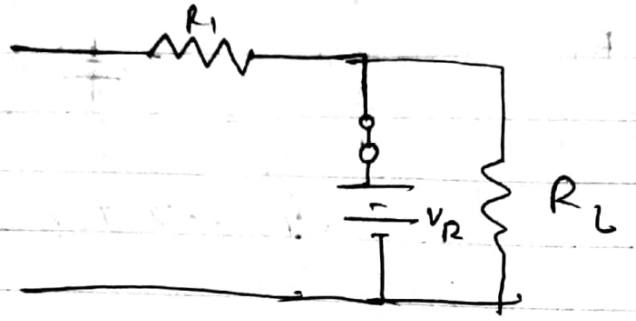




★ Parallel clipper with reference voltage V_R

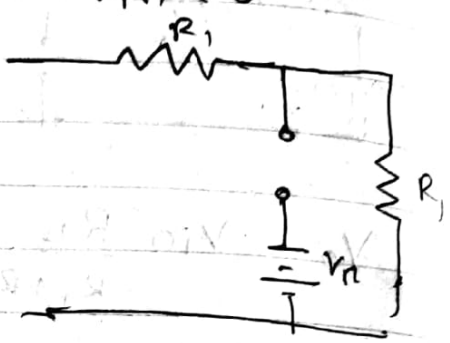


$V_{in} > 0$

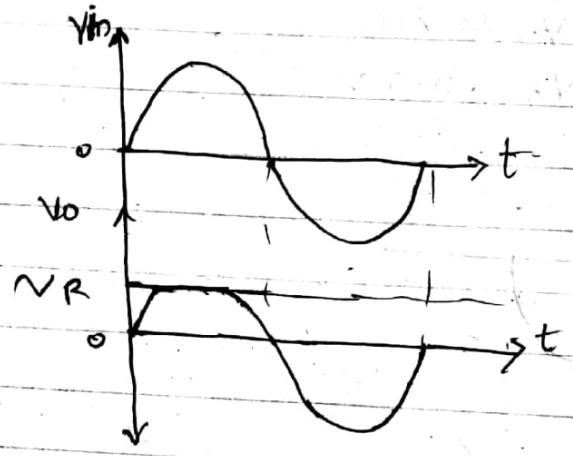


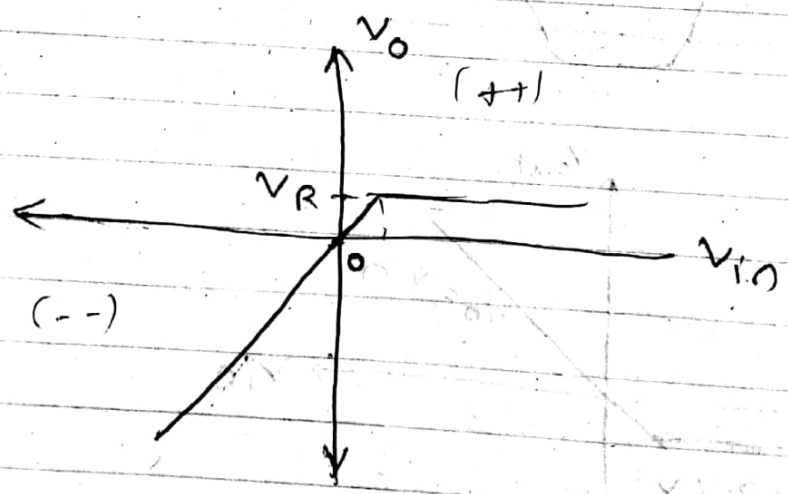
$V_o = V_R$

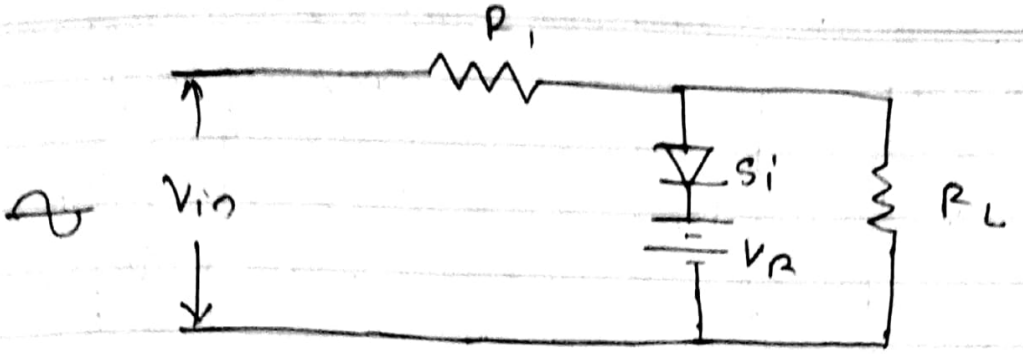
$V_{in} < 0$



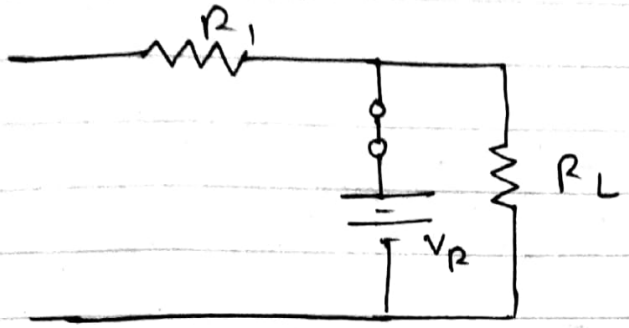
$V_o \simeq V_{in}$







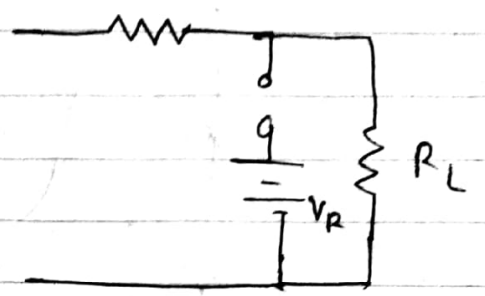
$V_{in} > 0$



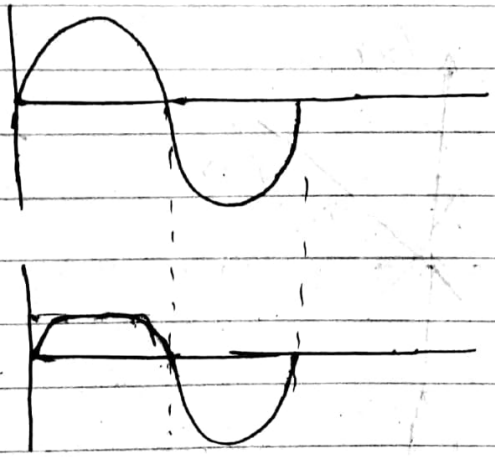
$V_R = 2 - V_\varphi$

$V_o = V_R + 0.7$

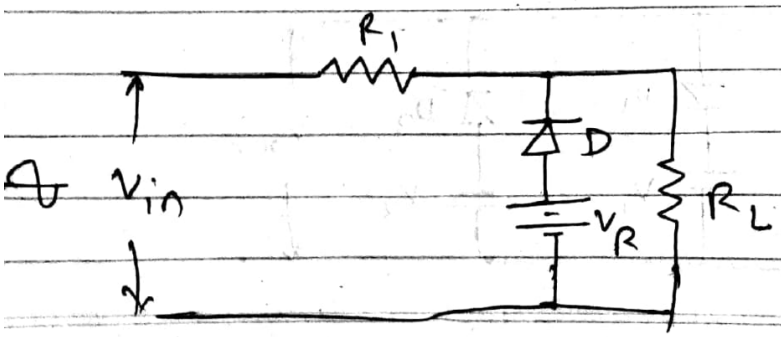
$V_{in} < 0$

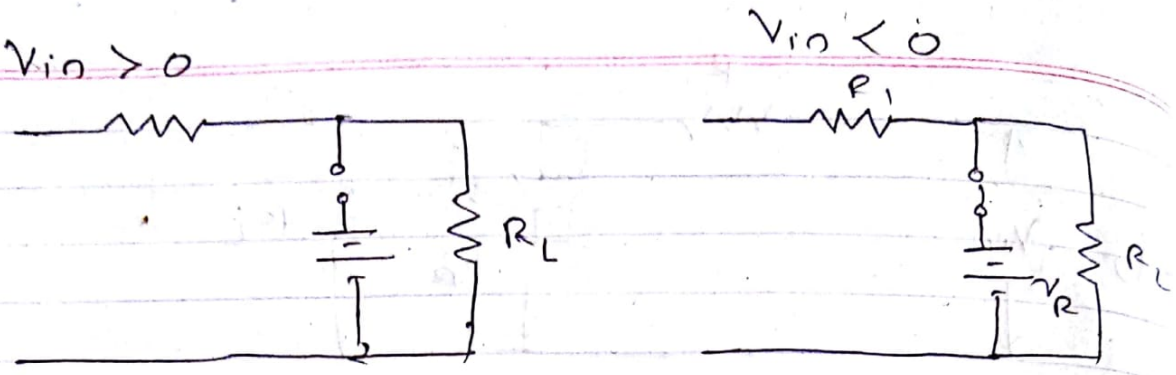


$V_o \simeq V_{in}$

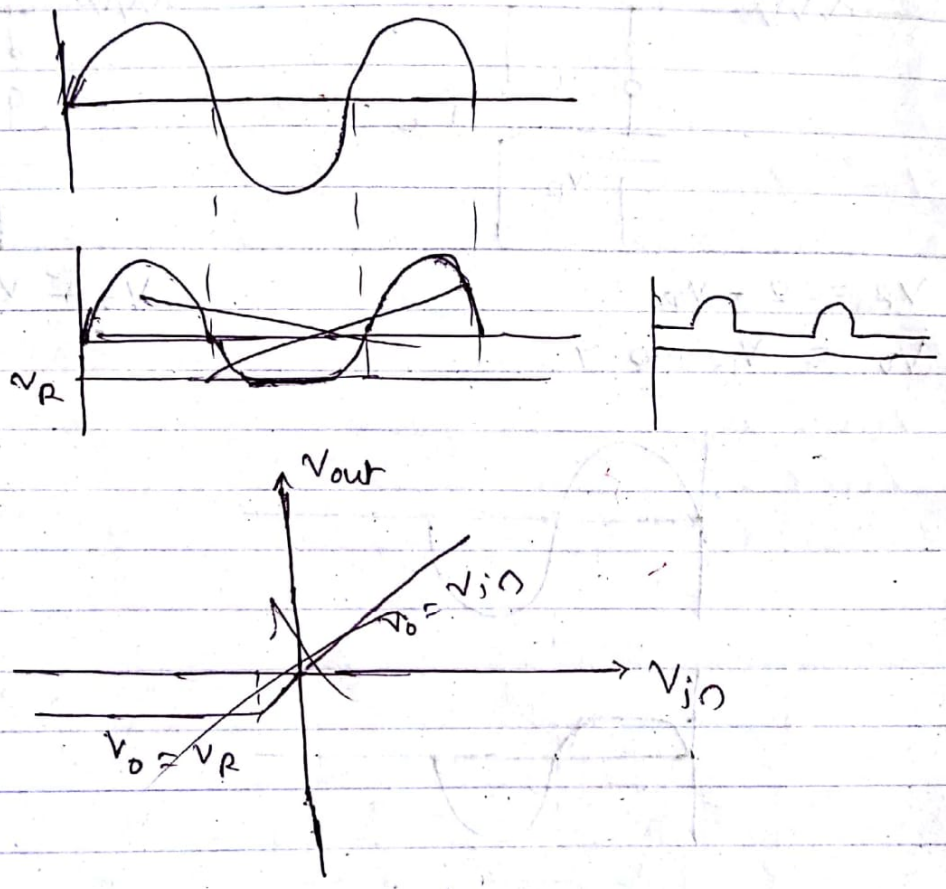


★ Parallel clipper with reference voltage V_R Negative clipping



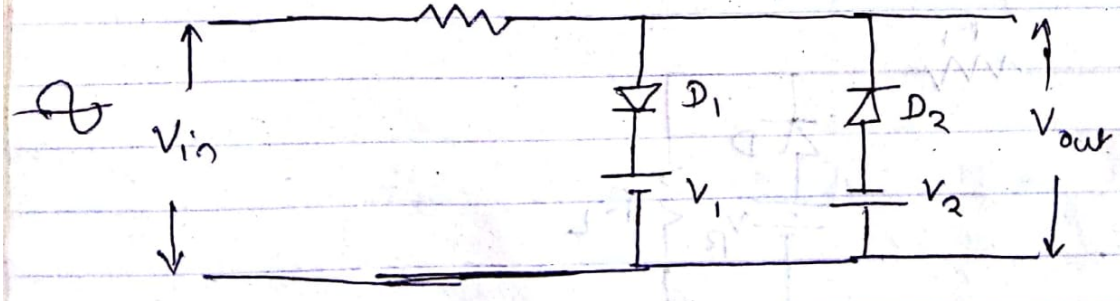


$V_o \simeq V_{in}$ $\qquad$ $V_o = V_R$



Combination of clipping

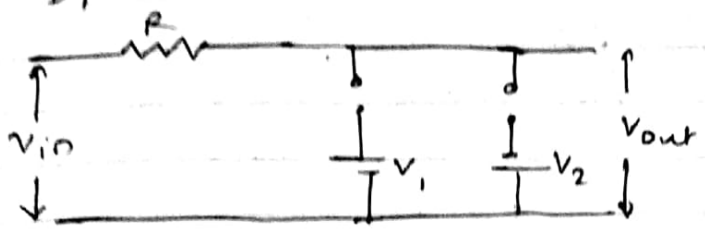
★ Two way $//^{ly}$ R clipper



+ve half cycle

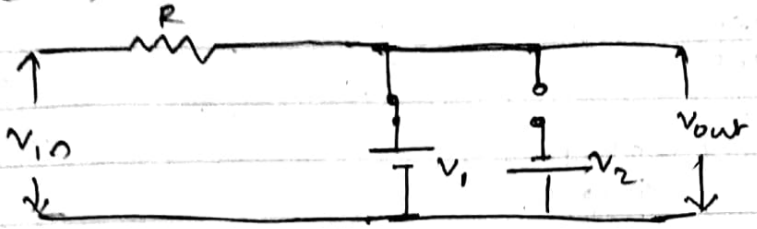
Case i) $0 < V_{in} < V_1$

D_1 - R.B $\qquad$ D_2 - R.B



$V_{out} = V_{in}$

Case ii) $V_{in} > V_1$

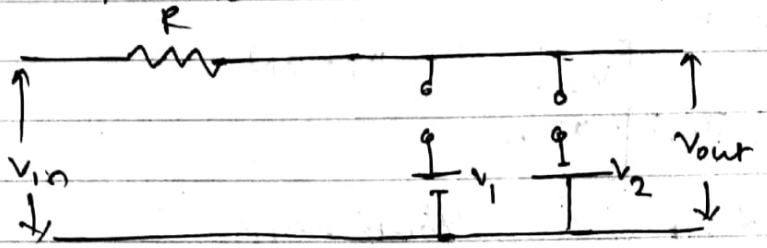


$V_{in} = V_1$

-ve half cycle.

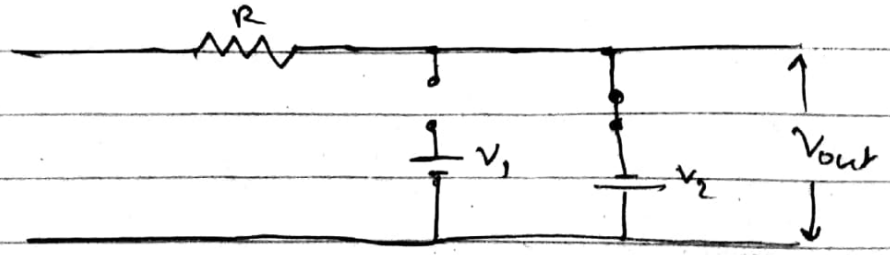
Case iii) $0 > V_{in} > V_2$

D_1 - R.B $\qquad$ D_2 - R.B

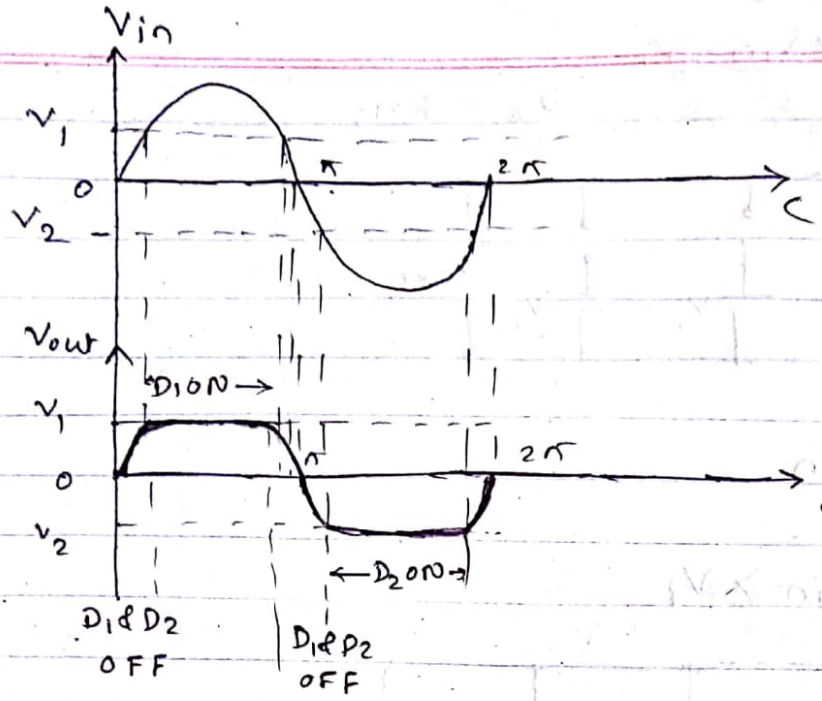


$V_{out} = V_{in}$

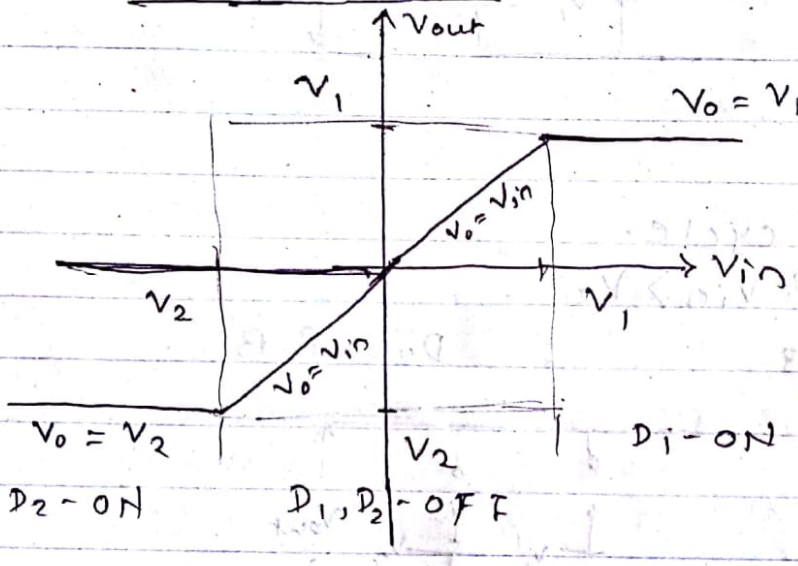
Case iv) $V_{in} < V_2$



$V_{out} = V_2$



*Transfer characteristic



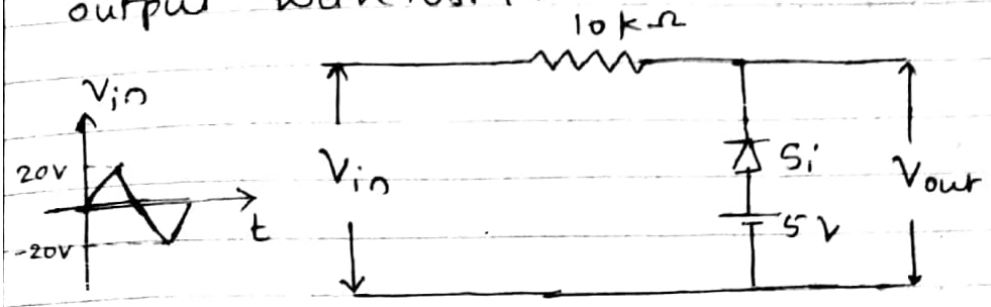
+ve $0 < V_{in} < V_1$ $V_{out} = V_{in}$

$V_{in} > V_1$ $V_{out} = V_1$

-ve $0 > V_{in} > V_2$ $V_{out} = V_{in}$

$V_{in} < V_2$ $V_{out} = V_2$

1) For the ckt shown below determine the transfer characteristic and sketch the output waveform.

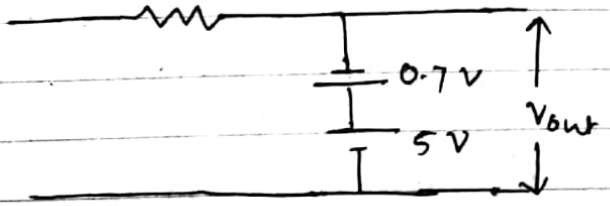


Soln:-

Case i) As the given diode is Silicon diode then, cutting voltage

$V_\gamma = 0.7V$

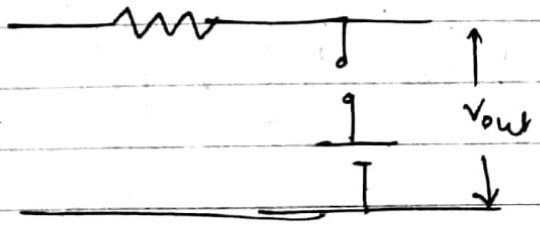
case i) $0 < V_{in} < 5V$



$V_{out} = 5 - 0.7$

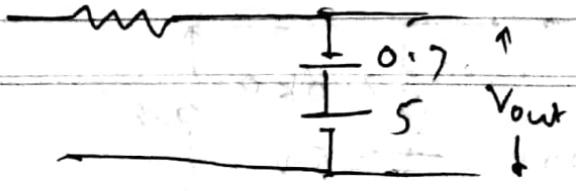
$V_{out} = 4.3V$

case ii) $V_{in} > 5V$

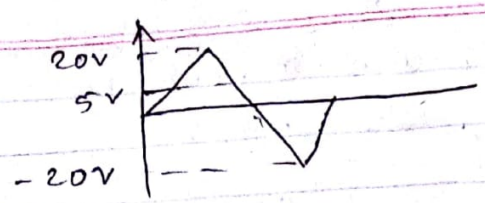


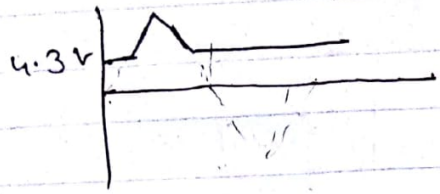
$V_{out} = V_{in}$

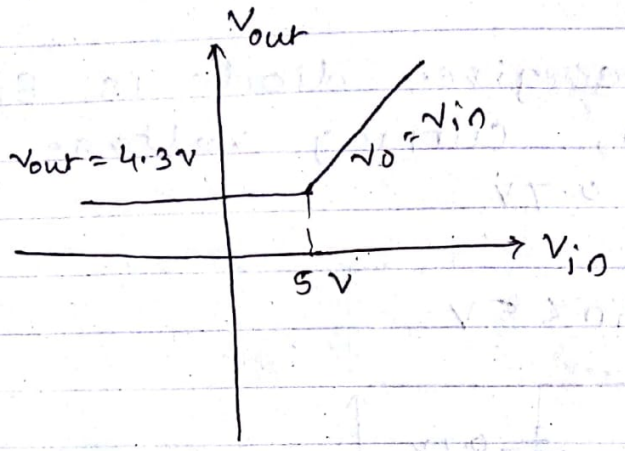
Case iii) $V_{in} < 0$



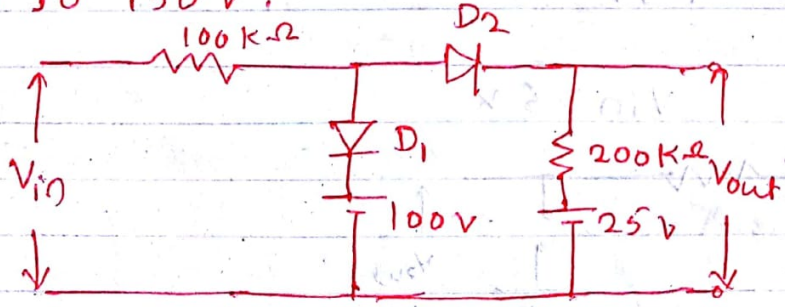
$V_{out} = 4.3V$







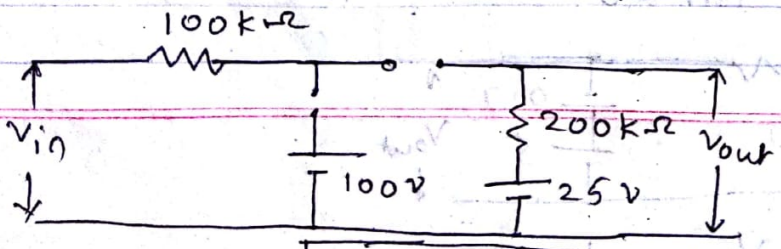
2] For the clipper ckt shown obtain its transfer characteristic. Assume ideal diodes. The input varies linearly from 0V to 150V.



Soln:-

Case i) $0 < V_{in} < 25V$

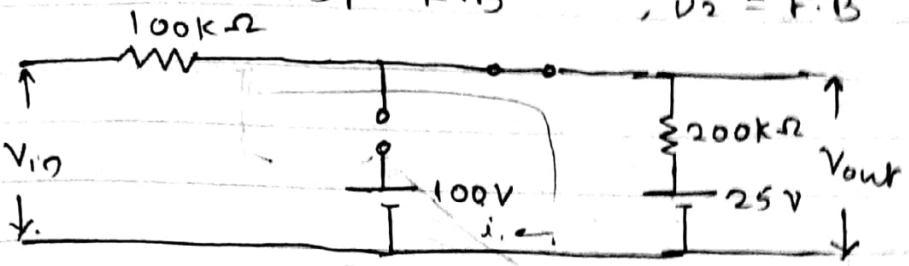
D_1 - R.B D_2 - R.B.



$V_{out} = 25V$

case ii) $25 < V_{in} < 100$

D_1 - R.B , D_2 = F.B



$$25 + (100 + 200)\,i = V_{in}$$

$$i = \frac{V_{in} - 25}{300\ k\Omega}$$

$$V_{out} = 25 + i \times 200$$

$$V_{out} = 25 + \frac{V_{in} - 25}{300\ k\Omega} \times 200\ k\Omega$$

$$V_{out} = 25 + \frac{2V_{in}}{3} - \frac{50}{3}$$

$$V_{out} = \frac{25}{3} + \frac{2V_{in}}{3} \quad \text{— (1)}$$

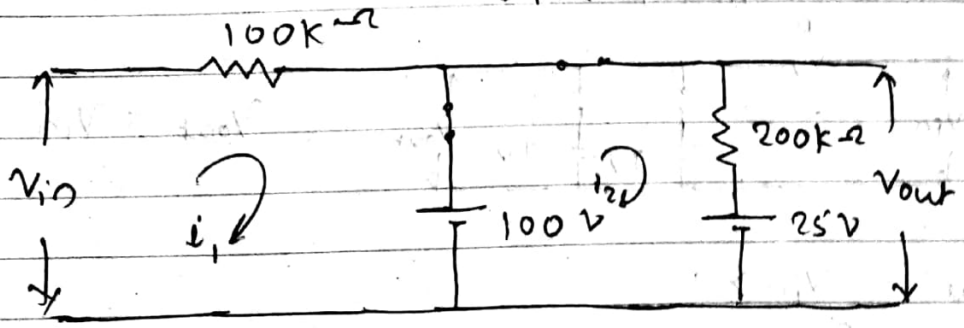
$V_{in} = 25\ V$, $V_{out} = 25\ V$

$V_{in} = 50\ V$ $V_{out} = 41.6\ V$

$V_{in} = 100\ V$ $V_{out} = 75\ V$

Case iii) $100 < V_{in} < 150$

D_1 & D_2 are F.B



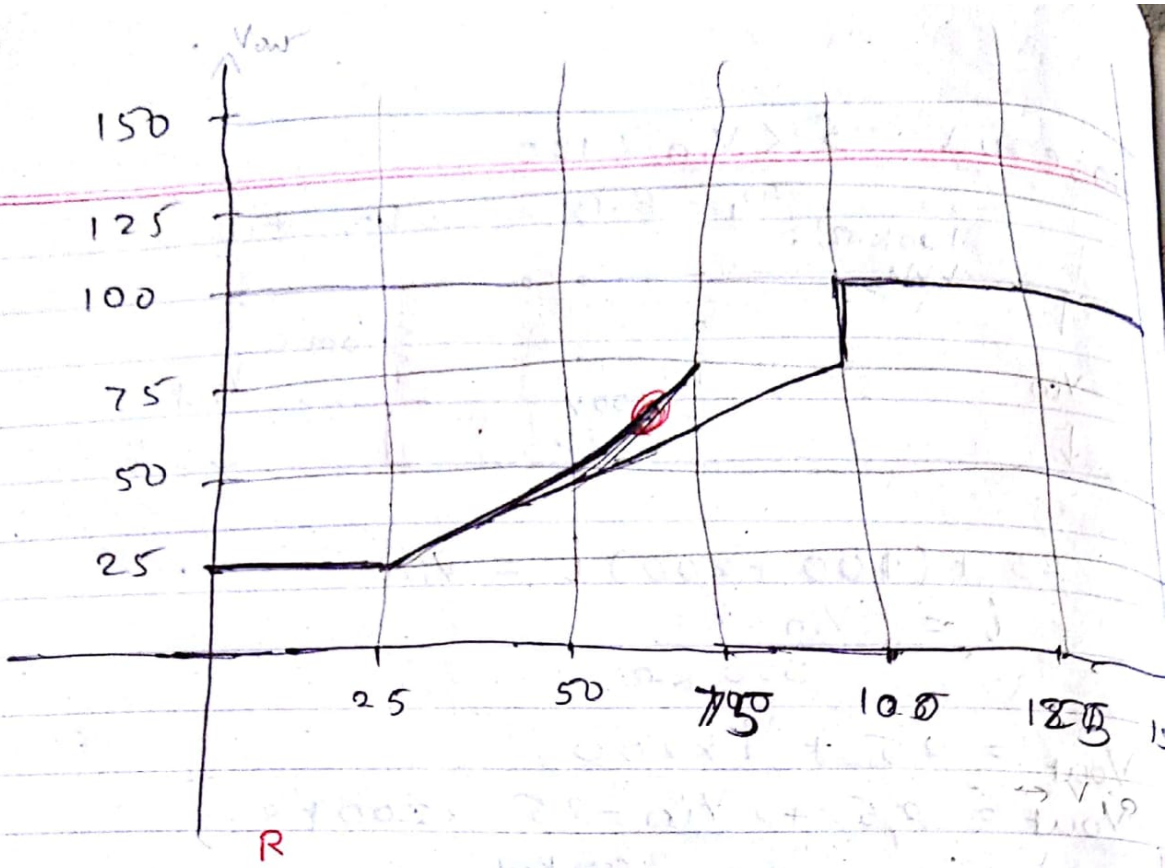
loop ② $25 + 200k\Omega\, i_2 = 100$ — (1)

loop ① $100k\Omega\, i_1 + 100 = V_{in}$ — (2)

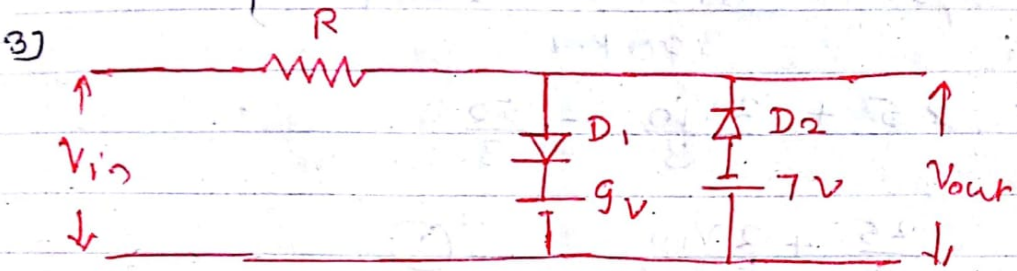
$V_{out} = (200k\Omega)\, i_2 + 25$ — (3) $i_2 = \frac{100 - 25}{200k\Omega}$

$V_{out} = 200 \times 0.375 + 25$ $i_2 = 0.375\ mA$

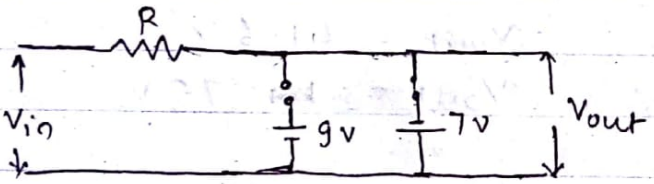
$V_{out} = 100V$



3)

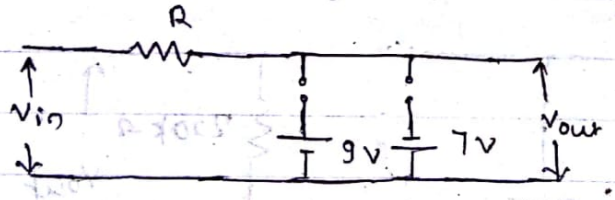


Case i) $0 < V_{in} < 7$



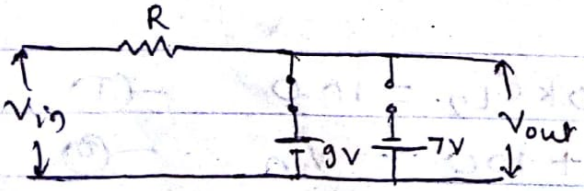
$V_{out} = 7V$

Case i) $7 < V_{in} < 9$



$V_{out} = V_{in}$

Case iii) $V_{in} > 9$



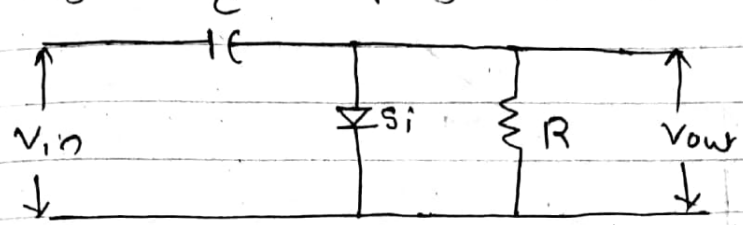
$V_{out} = 9V$

Case iv) $V_{in} < 0$

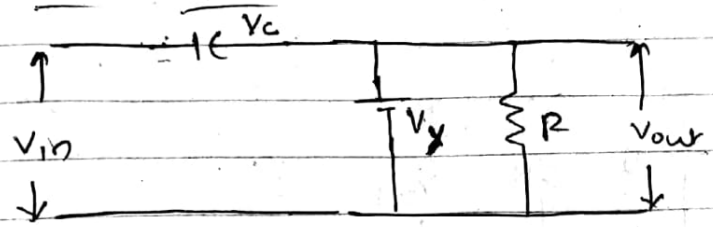
* Clampers :-

It is used to add d.c level of clampers circuit.

* Negative Clamping ckt.



+ve half cycle



$$V_y + V_c = V_{in}$$

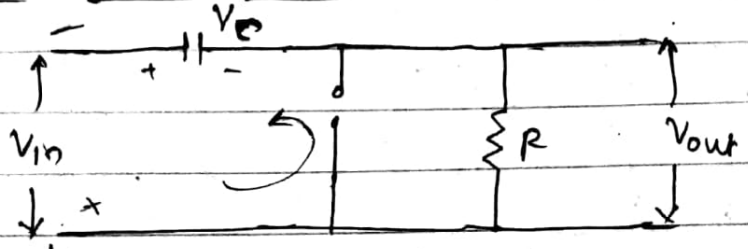
$$V_c = V_{in} - V_y$$

During +ve half cycle capacitor acts as a battery.

Applying KVL

$$V_c = V_{in} - V_y$$

-ve half cycle



D $\pm$ R.B.

Capacitor start discharging through R

$$-V_{in} + V_{out} + V_c = 0$$

$$V_{out} = -V_c + V_{in}$$

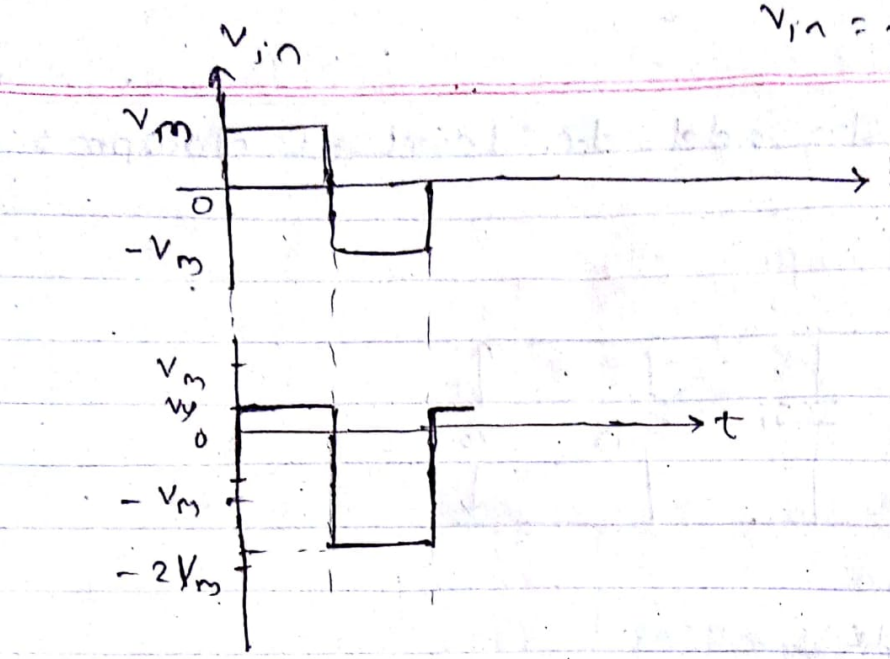
$$V_{out} = V_{in} - V_c$$

$$V_{out} = V_{in} - (V_m - V_y)$$

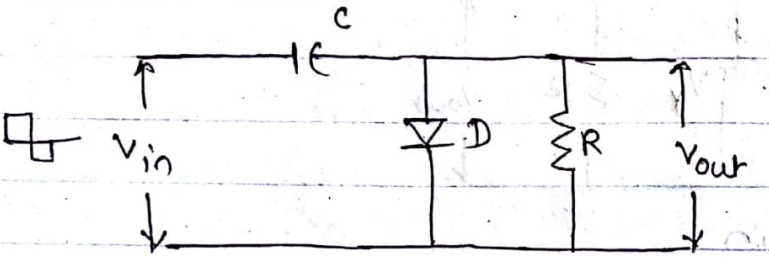
$V_{in} = 0 \quad V_o = V_y - V_m$

$V_{in} = V_m \quad V_o = V_y$

$V_{in} = -V_m \quad V_o = V_y - 2V_m$

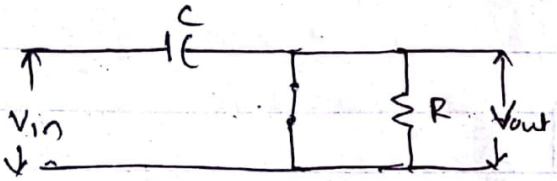


Ideal diode



+ve half cycle

D → F.B

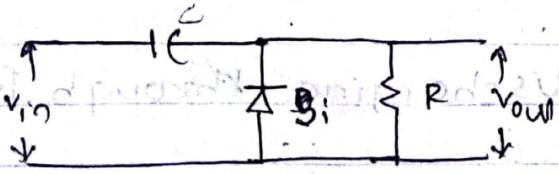


~~$V_{out} = 1$~~ $\quad \boxed{V_c = V_{in}}$

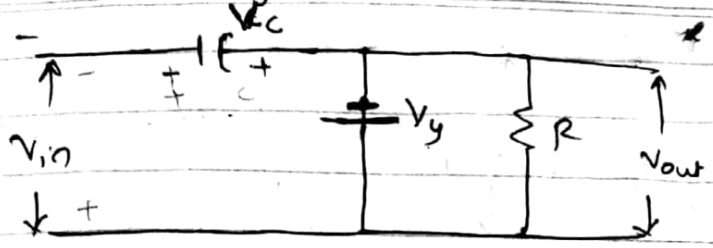
For $V_{in} = V_m$

$\boxed{V_c = V_m}$

* Positive clamper



-ve half cycle



$-V_y + V_c + V_{in} = 0$

$V_c = V_{in} + V_y$

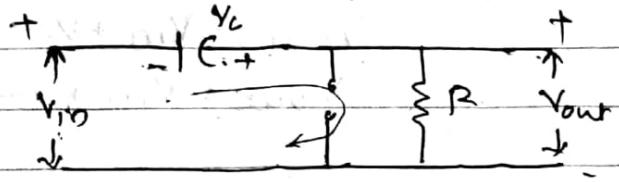
for $V_{in} = V_m$

$V_c = V_m + V_y$

$V_{in} + V_c - V_y = 0$

$V_c = V_y - V_{in}$

+ve half cycle



$V_{out} - V_{in} - V_c = 0$

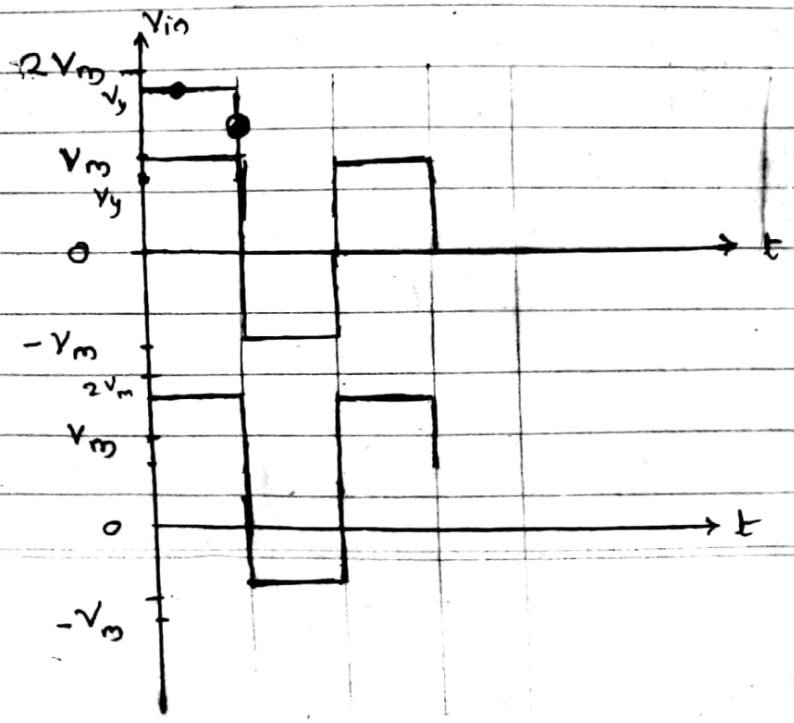
$V_{out} = V_{in} + V_c$

$V_{out} = V_{in} + (V_m - V_y)$

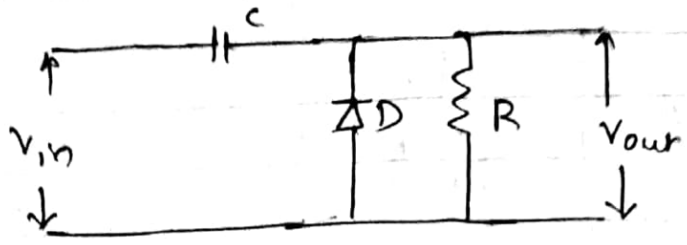
$V_{in} = 0V$ $\quad V_o = V_m - V_y$

$V_{in} = V_m$ $\quad V_o = 2V_m - V_y$

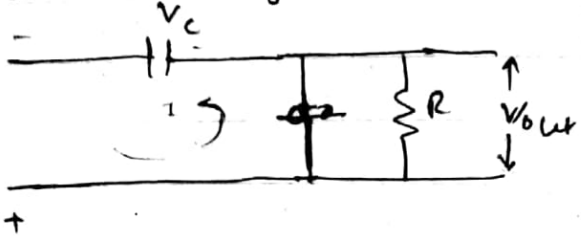
$V_{in} = -V_m$ $\quad V_o = -V_y$



Positive clamper for ideal diode



-ve half cycle



$-V_{in} + V_c = 0$

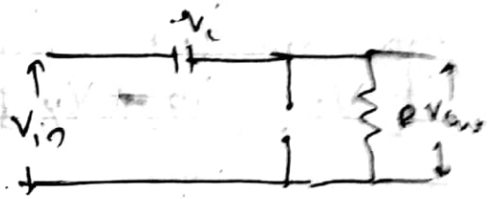
$V_c = V_{in}$

for $V_{in} = V_m$

$V_c = V_m$

+ve half cycle

D - OFF



$V_{out} = V_{in} + V_c$

$V_{out} = V_{in} + V_m$

$V_{in} = -V_m$

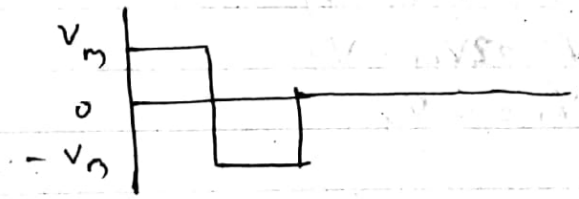
$V_{in} = 0$

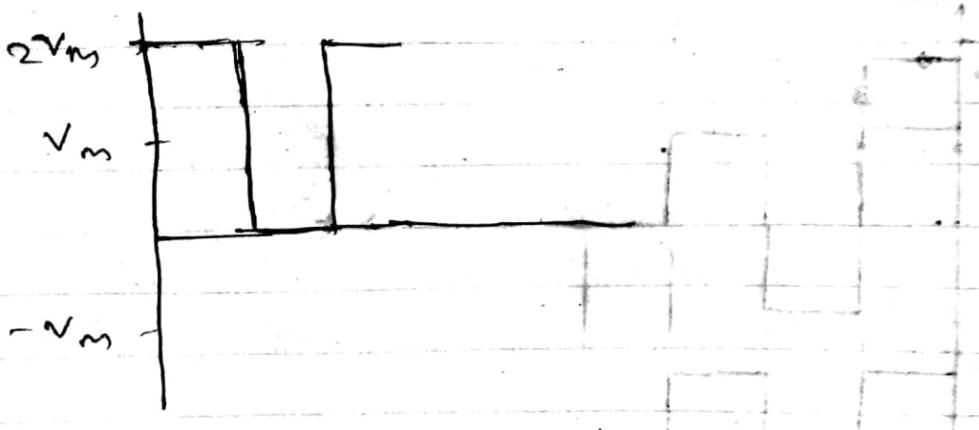
$V_{in} = V_m$

$V_o = 0$

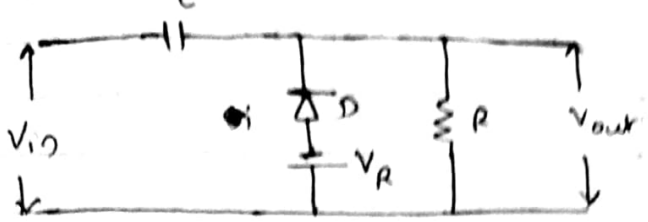
$V_o = V_m$

$V_o = 2V_m$



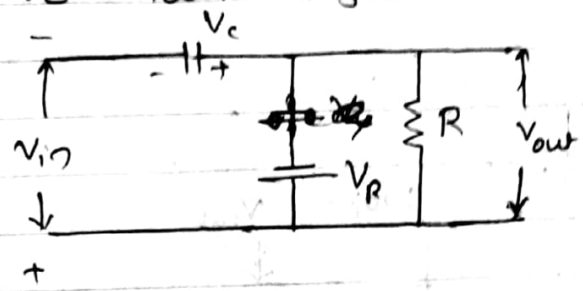


Positive clamper with battery



The addition of D.C. level and the shape of the o/p waveform can be control by adding additional voltage source in series with the diode.

-ve half cycle.



+

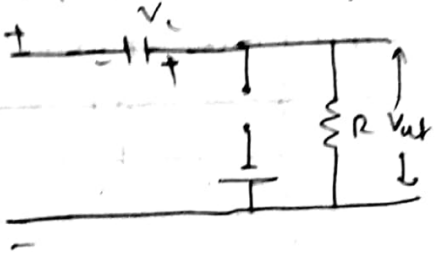
$-V_{in} + V_R + V_c = 0$

$V_c = V_{in} - V_R$

for $V_{in} = V_m$

$$V_c = V_m - V_R$$

+ve half cycle



$V_{out} - V_c - V_{in} = 0$

$V_{out} = V_c + V_{in}$

$$V_{out} = V_{in} + (V_m - V_R)$$

$V_{in} = -V_m$

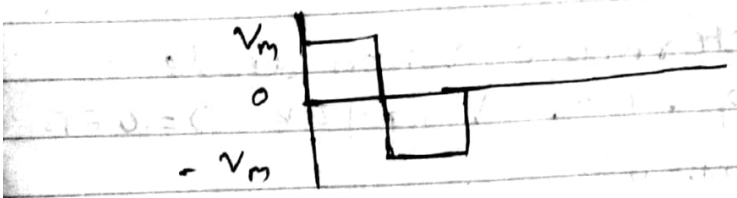
$V_{in} = 0$

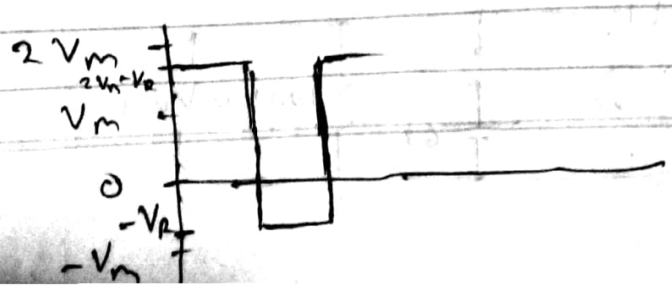
$V_{in} = V_m$

$V_o = -V_R$

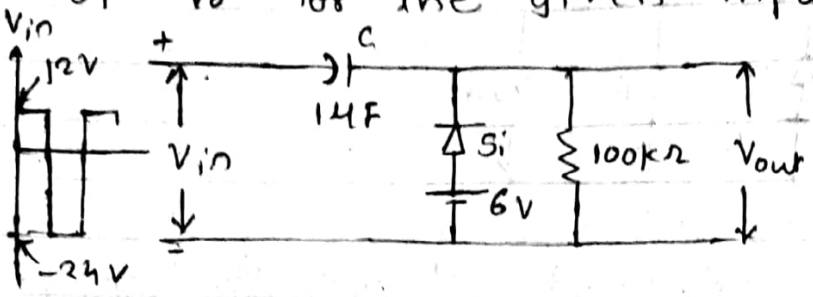
$V_o = V_m - V_R$

$V_o = 2V_m - V_R$





1) For the ckt. shown below plot the waveform of V_o for the given input.

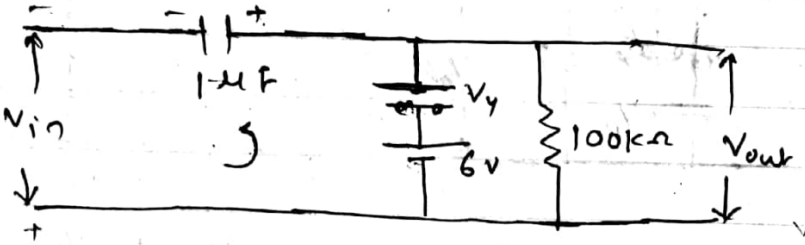


f = 1kHz

Soln:-

Step:- Find capacitor voltage V_c when diode is 'ON'.

When $V_{in} = -24V$ the diode is conducting. Capacitor starts charging



$$-V_{in} - 6 + V_y + V_c = 0$$

$$V_{in} = V_c + V_y - 6$$

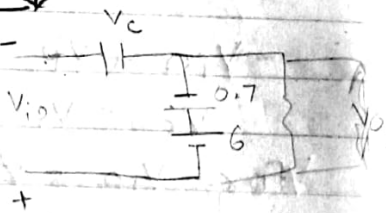
$$V_c = V_{in} - V_y + 6$$

$$V_c = -24 - 0.7 + 6$$

$$V_c = -V_{in} + 5.3$$

$$V_c = -(-24) + 5.3$$

$$V_c = 29.3\ V$$



$-V_{in} - 6 + 0.7 + V_c = 0$

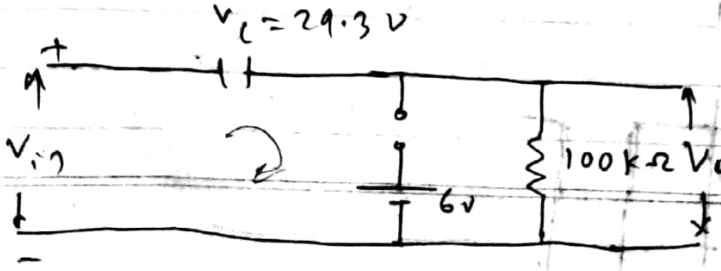
$V_c = 5.3 + V_{in}$

$V_i - V_c - 0.7 + 6V = 0$

$V_i = V_{in} - 5.3$

$V_i - 5.3 = V_c$

Step 2: O/p is determine when diode is not conducting. i.e. $V_{in} = 12V$ D = OFF.



$-V_c + V_{out} - V_{in} = 0$

$V_{out} = V_{in} + V_c$

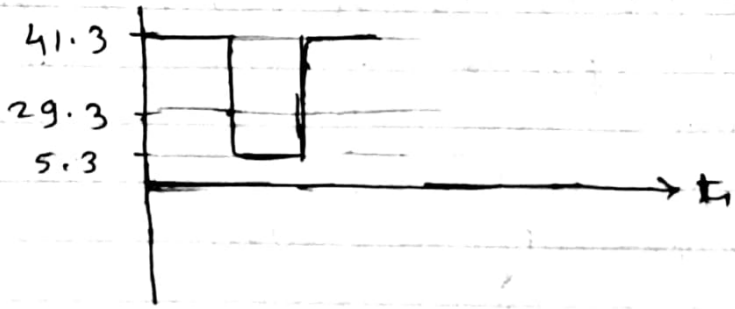
$= 12 + 29.3$

$V_{out} = 41.3\,V$

$V_{in} = 0\,V$ $\quad V_o = 29.3\,V$

$V_{in} = 12\,V$ $\quad V_o = 41.3\,V$

$V_{in} = -24\,V$ $\quad V_o = 5.3\,V$



2]

From Given:-

$V_{in} = 20\,V$ $\quad V_o = 30\,V$

$V_{in} = -20\,V$ $\quad V_o = -10\,V$

$V_{in} = 0\,V$ $\quad V_o = 10$

+ve half cycle

$V_o = 20 + V_c$

$30 = 20 + V_c$

$V_o = V_{in} + V_c$

$V_c = V_m + V_R + V_y$

$V_c = 20 + V_R - V_y$

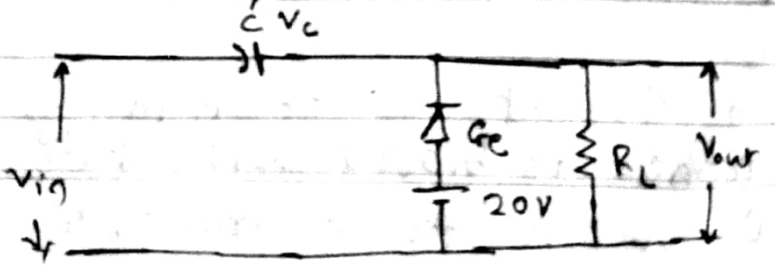
-ve half cycle

$V_{in} = -20$ $\quad V_o = -10$

$V_{in} = V_c + V_R$

$V_{in} = V_c + V_R$

$V_{in} = 20 + 2V_R - V_y$

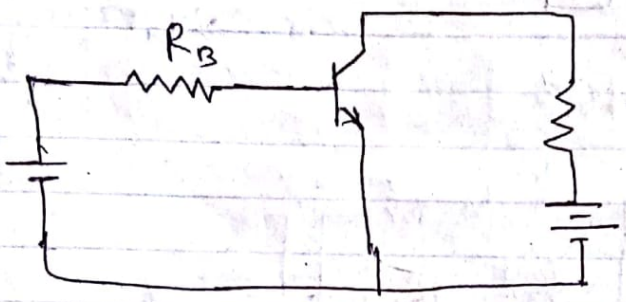


* Transistor Biasing *

Biasing

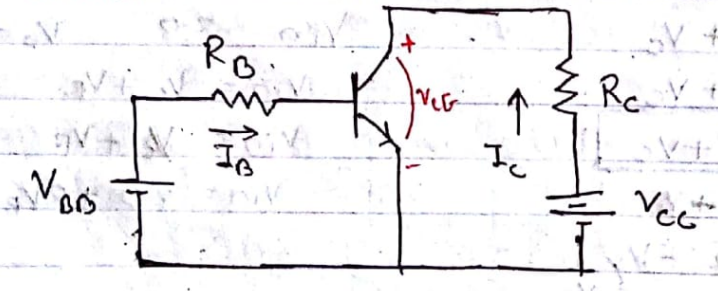
To operate transistor in desired region we need to apply external d.c. vtg. of correct polarity & magnitude to the 2 junction of tran^r this is called the biasing of transistor.

Whe tran^r. is bias it establishes some current & vtg. conditions these cond^n are known as operating cond^n or dc operating points or quiescent point or q-point



For proper operation of trans. the operating point must stable with a change in trans. parameters the operating points also shift

DC Load Line



Consider a CE ckt. as shown in fig.

The trans. is biased with two supply vtg. V_{BB} & V_{CC}. to drive trans. in active region. BE junction should be F.B biase and CE jun —— " —— R.B ——.

Applying KVL to collector ckt.

$V_{cc} = I_c R_c + V_{CE}$ —①

where $I_c R_c$ is vrg. drop across resistor R_c

$I_c = \frac{V_{cc} - V_{CE}}{R_c}$ —②

Comparing eq^n ② with eq^n of straight line $y = mx + c$ where m - slope & c - intersept point on y-axis.

We can draw a straight line on graph of I_c & V_{CE} with slope $(-1/R_c)$ and c - y axis intersept at (V_{cc}/R_c)

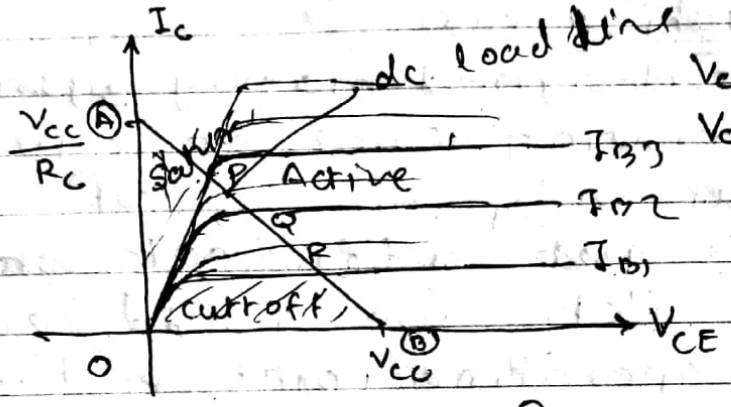


fig shows o/p char- of CE configuration bet^n point A & B a line is drawn it is called as dc load line - Dc load line is a plot of I_c & V_{CE} for given value of R_c & V_{cc}.

If one parameter out of I_c, V_{CE} & I_B is known other parameters can be determine using d.c. load line. The slop of the line depends on the value of R_c.

Applying KVL to the base ckt.

$V_{BB} - I_B R_B - V_{BE} = 0$

$I_B = \frac{V_{BB} - V_{BE}}{R_B}$

If we draw characteristic of I_B on o/p characteristic, it intersepts with d.c load line.

And that intersection point is called as Q. In fig. for different values of I_B we get different intersection point such as P, Q & R all these points are Q point.

* Selection of Q-point

1) Near to saturation region
2) Near to cut off region
3) exact at the center of D.C L.L.

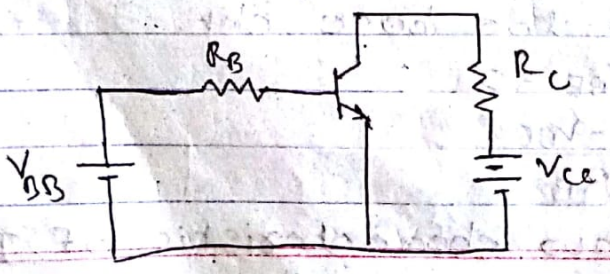
* Bias stabilization

We designed biasing system to fixed operating point at centre of act region but only fixing of operating region is not sufficient while design a biasing ckt. we should take care that the operating point will not shift into undesirable region. while designing biasing ckt. following two factors are consider which are responsible for the shifting of operating point.

1) Temperature 2) β_{dc} (d.c. gain of tra

* Biasing circuit

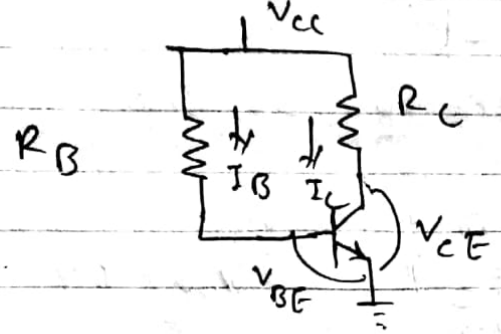
Typical biasing circuit



Here Emitter base junction is forward bias by V_{BB} & C-B junction is reverse using V_{cc}

The required value to make transistor conducting $V_{BE} = 0.7V$ but it is diff^{n} to have a battery of 0.7V. So the resistor R_B is connected in series with V_{BB} Now R_B is adjested according to required V_{BB}.

Fixed bias circuit.



Here V_{cc} is the Fixed value once R_B is selected I_B also fixed to a same value hence the circuit is called fixed bias ckt.

Applying KVL to the Base ckt.

$$V_{cc} = I_B R_B + V_{BE} \quad \text{— (1)}$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

As $V_{BE} << V_{cc}$

$$I_B = \frac{V_{cc}}{R_B}$$

KVL to the collector ckt

$$V_{cc} = I_C R_C + V_{CE} \quad \text{— (2)}$$

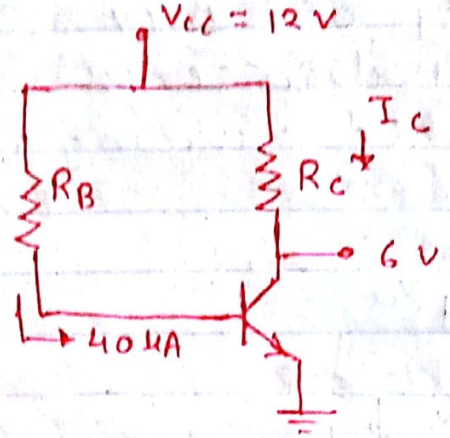
For C-E configuration

$$I_c \simeq \beta I_B$$

$\therefore$ (2) $\Rightarrow$ $I_c = \frac{V_{cc} - V_{CE}}{R_C}$

$$\beta I_B = \frac{V_{cc} - V_{CE}}{R_C}$$

For the fixed bias ckt. shown determine collector current I_C, R_C, R_B, V_{CE}



& Assume $\beta = 80$, $V_{BE} = 0.7$

$I_B = 40\mu A$ $V_{BE} = 0.7$ $V_{CE} = 6V$

$V_{CC} = 12V$ $\beta = 80$

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$-R_B = \frac{V_{BE} - V_{CC}}{I_B}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.7}{40 \times 10^{-6}} = 28.25 \times 10^4$$

$$R_B = 282.5\ K\Omega$$

$$I_C = \beta I_B$$

$$I_C = 80 \times 40 \times 10^{-6}$$

$$I_C = 3.2\ mA$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12 - 6}{3.2 \times 10^{-3}} = 1.875\ K\Omega$$

2] For the fixed bias ckt. $R_B = 50\ K\Omega$, $R_C = 500\ \Omega$ $V_{CC} = 10V$. Find the co-ordinates of the operating point draw d.c load line & locate the operating point on it. Assume Si trans^r with $\beta = 50$ & $V_{BE} = 0.7V$

$I_C = \beta I_B$

$I_C = 50 \times 0.186 \times 10^{-3}$

$\boxed{I_C = 9.3 \text{ mA}}$

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$

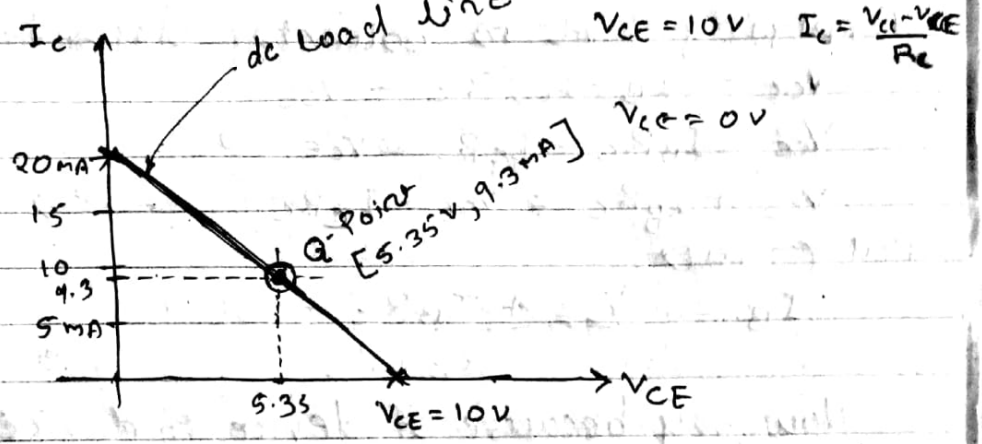
$I_B = \frac{10 - 0.7}{50 \times 10^3}$

$I_B = 0.186 \text{ mA}$

$V_{CE} = V_{CC} - I_C R_C$

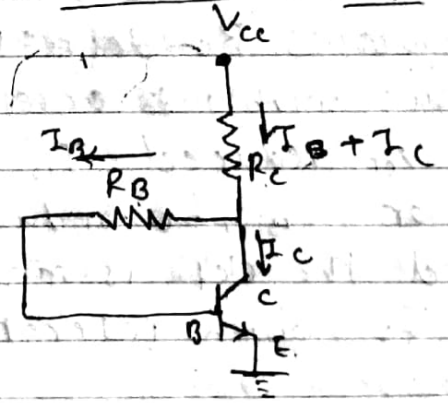
$= 10 - 9.3 \times 10^{-3} \times 500$

$\boxed{V_{CE} = 5.35 \text{ V}}$



⇒ Collector feedback bias circuit.

C to B bias ckt. is an improvement over fixed bias ckt



R_B is connected to 'C' instead of V_{CC}.

Here we can see that the biasing resistance R_B is connected between 'C' & 'B'. I_B flows through R_B & $I_C + I_B$ flows through R_C

Let us analyse:

Applying KVL to Base ckt.

$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$

$V_{CC} = (R_C + R_B) I_B + I_C R_C + V_{BE}$

$$I_B = \frac{V_{cc} - I_c R_c - V_{BE}}{R_B + R_c} \quad \text{— (1)}$$

KVL to collector

$$I_c = \beta I_B$$

$$\frac{I_c}{\beta} = \frac{V_{cc} - I_c R_c - V_{BE}}{R_B + R_c}$$

$$I_c = \beta \frac{[V_{cc} - I_c R_c - V_{BE}]}{R_B + R_c}$$

Applying KVL to collector circuit.

$$V_{cc} = (I_B + I_c) R_c + V_{CE}$$

$$V_{cc} - I_B R_c - I_c R_c - V_{CE} = 0$$

$$V_{CE} + I_B R_c = V_{cc} - I_c R_c \quad \text{— (2)}$$

Put (2) in (1)

$$I_B = \frac{V_{CE} + I_B R_c - V_{BE}}{R_B + R_c}$$

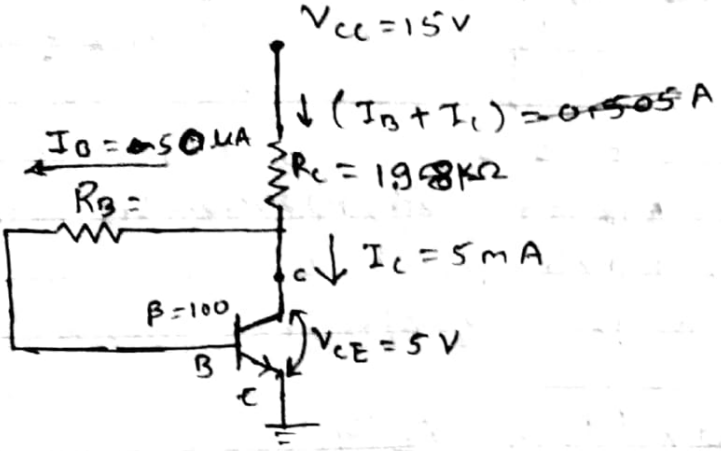
Now say because of device to device change 'β' value or because of change in temp the 'C' current increases. Because of increase in I_c volt. drop across R_c ~~decreases~~ increases as V_{cc} is const. value with increament in I_c V_{CE} reduces. As V_{CE} reduced I_B also reduces. Also I_c depends on I_B, I_c reduces.

In other word the ckt. is maintaining a stable value of I_c which in turn stable Q-pt. point position.

Here in the ckt. R_B is directly connected across I/p (B) and O/p (C) i.e. a part of O/p is sent back to the I/p.

An increament in I_c decreases I_B i.e. -ve feedback exist in the ckt. So this ckt is called collector feedback biasing circuit.

1) For a given conditions of $V_{CC} = 15V$, $V_{CE} = 5V$, $I_C = 5mA$ & $\beta = 100$ design a collector to base bias ckt.



$I_C = \beta I_B$

$I_B = \frac{5 \times 10^{-3}}{100}$

$I_B = 50\mu A$

$I_C + I_B = 50\mu A + 5mA =$

$R_B + R_C = \frac{V_{CC} - I_C R_C - V_{BE}}{I_B}$

$= 15 - 5 \times 10^{-3} \times R_C -$

$V_{CE} + I_B R_C = V_{CC} - I_C R_C$

$V_{BE} = 0.7$ for Si

$5 + 0.5 \times 10^{-5} R_C = 15 - 0.005 R_C$

$5 R_C = 10$

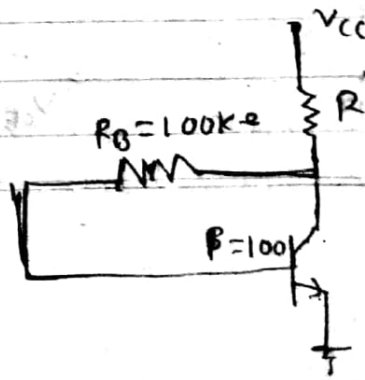
$R_C = 1.98K\Omega$

$I_B = \frac{V_{CE} + I_B R_C - V_{BE}}{R_B + R_C}$

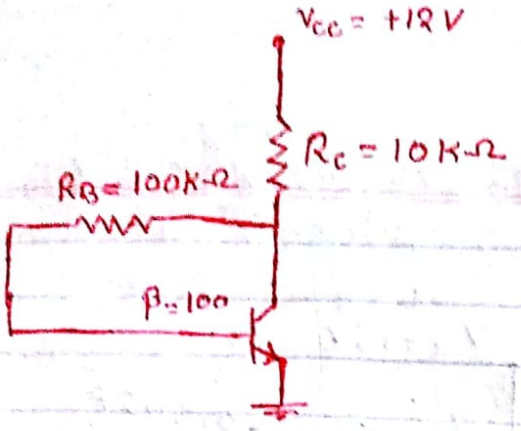
$50 \times 10^{-6} = \frac{5 + 50 \times 10^{-6} \times 1.98 \times 10^3 - V_{BE}}{R_B + 1.98 \times 10^3}$

$50 \times 10^{-6} R_B + 0.099 = 4.399$

$R_B = 86K\Omega$



2]



Assume for Si

$V_{BE} = 0.7$

$-V_{CC} + I_B R_C + I_C R_C + I_B R_B + V_{BE} = 0$

$-12 + 10000 I_B + 10000 R_C + 100000 I_B + 0.7 = 0$

$110K\, I_B + 10K\, I_C = 11.3$

$110K\, I_B = 11.3 - 10K I_C$ — (1)

$I_C = \beta I_B$

$I_C = 100 \times \frac{(11.3 - 10K I_C)}{110 \times 1000}$

$I_C = \frac{11.3}{1100} - \frac{100 \times 1000}{110 \times 10} I_C$

$10\, I_C = 10.27 \times 10^{-3}$

$I_C = 1.03\ mA$

(1) $\Rightarrow$ $110K\, I_B = 11.3 - 10K \times 1.03 \times 10^{-3}$

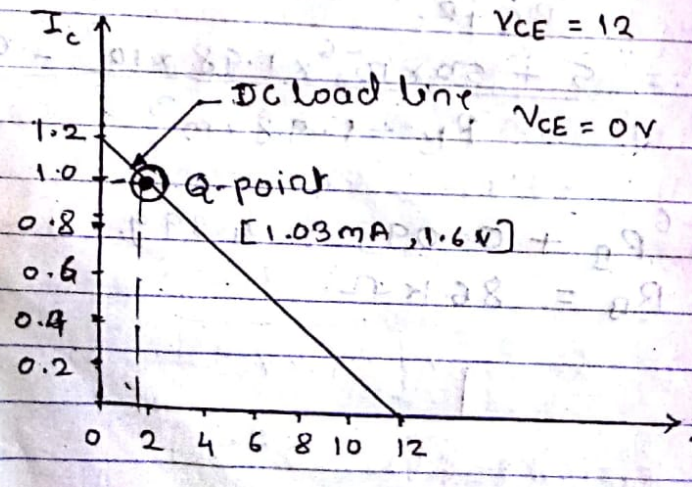
$I_B = 9.09\ \mu A$

$V_{CE} = V_{CC} - (I_B + I_C) R_C$

$V_{CE} = 12 - (9.09\mu + 1.03m)\, 10K$

$V_{CE} = 12 - 10.39$

$V_{CE} = 1.6\ V$



$V_{CE} = 12$ $I_C = \frac{V_{CC} - V_{CE}}{R_C} = 0$

$V_{CE} = 0V$ $I_C = 1.2\ mA$

★ Voltage Divider Bias Circuit :-

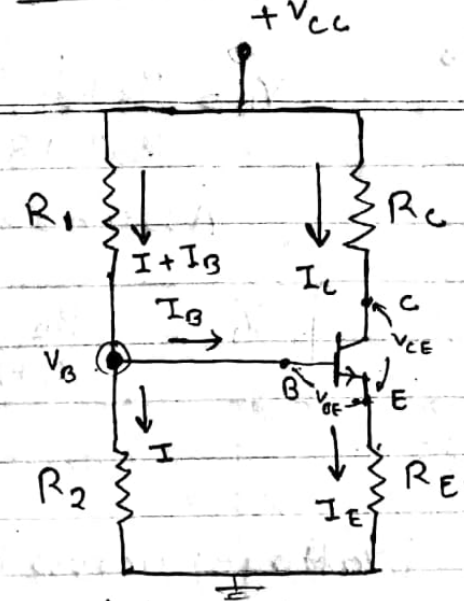


Fig. shows ckt. arrangement of VDB.C. Here biasing is provided by 3 Resistance R_1, R_2 & R_E. The resistors R_1 & R_2 act as potential divider which gives a fixed value of voltage at base terminal (V_B).

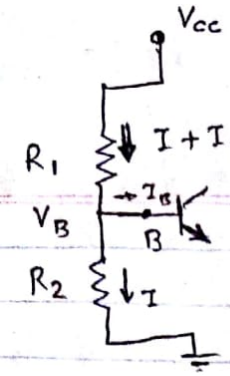
★ Operation:-

If I_C increases due to increament in temp. or change in β value the ammeter current I_E also increases which increases vtg. drop across R_E, Reducing voltage diff^n betⁿ base & emmiter (V_{BE}).

We know that base current dependson V_{BE}, with decreament in V_{BE} value I_B decreases as I_B decreases I_C decreases. This reduction in I_C compensets for change in I_C. From fig it is clear that ~~collector~~ voltage feedback exist in the emmiter bias ckt.

This is the most widly used method to provide biasing and stabilization.

★ Analysis :-

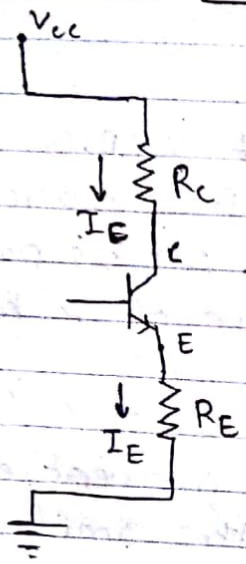


$$V_B = \frac{R_2 I'}{R_2 I + R_1 (I + I_B)} \cdot V_{cc}$$

Assume $I >> I_B$

$$\boxed{V_B = \frac{R_2}{R_1 + R_2} V_{cc}}$$

* Collector circuit:-



Voltage across R_E.

$$V_E = I_E R_E$$

$$V_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

KVL to collector ckt.

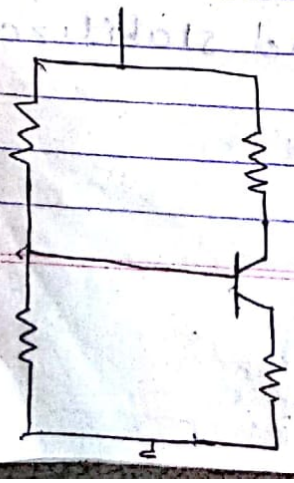
$$-V_{cc} + I_C R_c + V_{CE} + I_E R_E = 0$$

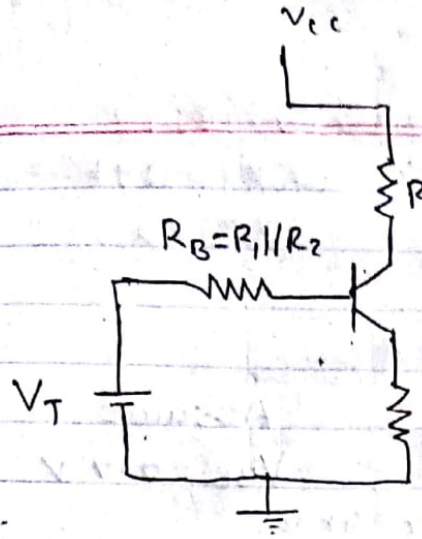
$$\boxed{V_{CE} = V_{cc} - I_C R_c - I_E R_E}$$

modify

$$\boxed{V_I = I_B R_B + I_E R_E + V_{BE}}$$

1] Find the co-ordinates of Q-point & locate it on the d.c load line for the vtg. divider ckt. Given:- $V_{cc} = 16\,V$, $R_1 = 62\,K\Omega$, $R_2 = 9.1\,K\Omega$, $R_c = 3.9\,K\Omega$, $R_E = 0.68\,K\Omega$, $\beta = 80$. The coupling capacitors are $10\,\mu F$. also find V_c, V_E & V_B.





Assume $V_{BE} = 0.7\,V$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} = 7.9\,k\Omega$$

$$V_T = V_{cc}\frac{R_2}{R_1+R_2} = \frac{16 \times 9.1}{62+9.1} = 2.04\,V$$

$$I_B = \frac{V_B - V_{BE}}{R_B} = \frac{2.04 - 0.7}{7.9} = 0.16\,mA$$

$I_C = \beta I_B$

$I_C = 80 \times$ $\quad (I_E = I_C + I_B)$

$$V_T = I_B R_B + I_E R_E + V_{BE}$$

$$I_B = \frac{V_T - I_E R_E - V_{BE}}{R_B} = \frac{2.04 - (80+1) I_B\, 0.68k - 0.7}{7.9k}$$

$$7.9k\, I_B = 1.34 - 55.08\, I_B$$

$$62.98\, I_B = 1.34$$

$$\boxed{I_B = 21.2\,\mu A}$$

$$I_C = \beta I_B = 80 \times 21.2\mu = 1.7\,mA$$

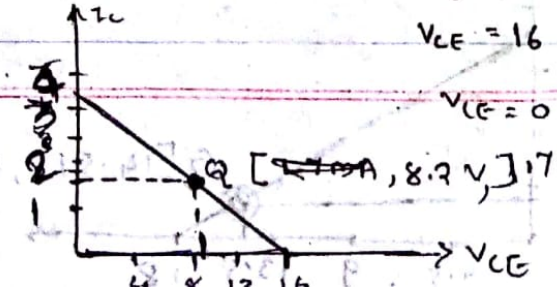
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = 16 - (1.7m)(3.9k) - (1.7m + 21.2\mu)\,0.68k$$

$$V_{CE} = 16 - 6.63 - 1.17$$

$$\boxed{V_{CE} = 8.2\,V} \qquad \boxed{I_C = 1.7\,mA}$$

$\boxed{V_E = 1.17\,V}$, $V_C = 5.63\,V$, $V_B = 0.17\,V$



$V_{CE} = 16 \quad I_C = \frac{V_{cc} - V_{CE}}{R_C + R_E} = 0V$

$V_{CE} = 0 \quad I_C = 3.5\,mA$

D.Soni

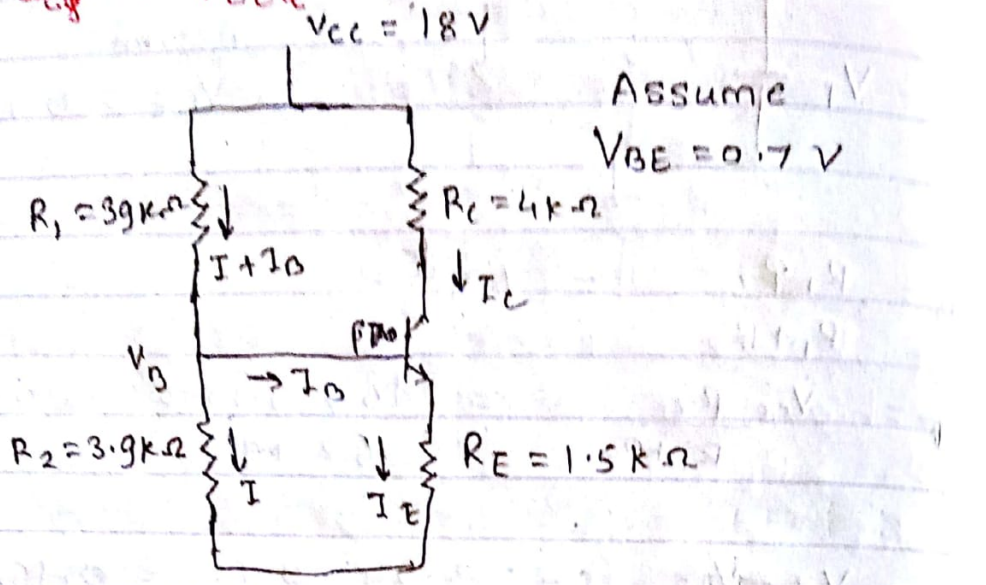
Ex-1

2] In a vtg-divider biased ckt (BJT)

$R_C = 4\,k\Omega$, $R_E = 1.5\,k\Omega$, $R_1 = 39\,k\Omega$

$R_2 = 3.9\,k\Omega$ $V_{CC} = 18\,V$ $\beta = 70$

Find I_{CQ} & V_{CEQ}



Assume

$V_{BE} = 0.7\,V$

Voltage across 'R_2'

$$V_B = \frac{R_2}{R_1+R_2} V_{CC} = \frac{3.9}{39+3.9} \times 18 = 1.63\,V$$

$$I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{1.63 - 0.7}{1.5\,k}$$

$$I_E = 0.62\,mA$$

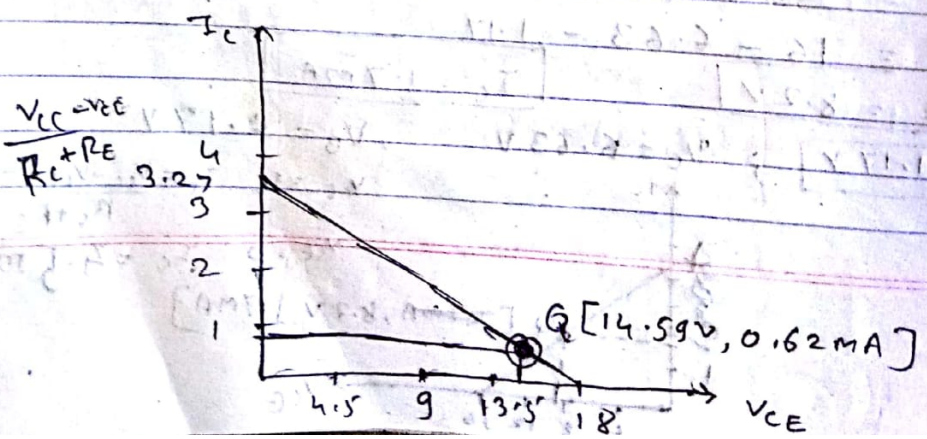
$I_E \simeq I_C$

$\therefore \boxed{I_C = 0.62\,mA}$

we've, $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

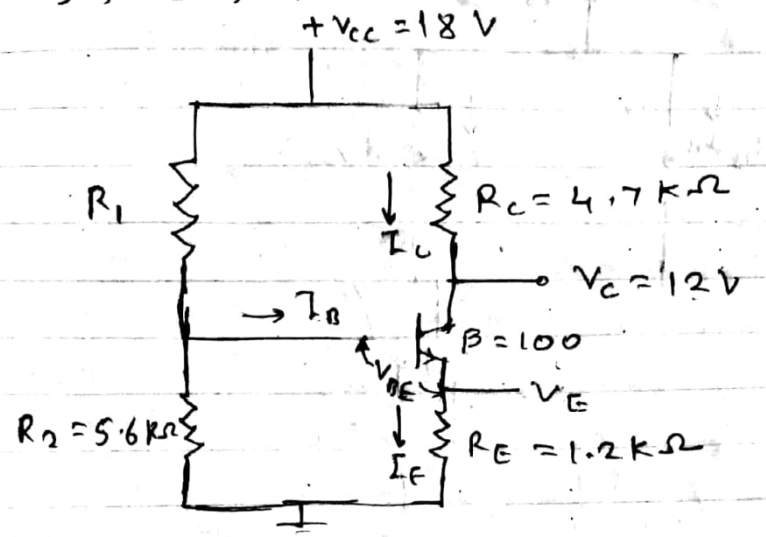
$= 18 - (0.62\,m \times 4k) - (0.62\,m \times 1.57k)$

$\boxed{V_{CE} = 14.59\,V}$



July-2014
07M

3] For the ckt. shown in the Fig. Find
I_C, V_B, V_E, R_1



$V_{BE} = 0.7$

$$I_C = \frac{V_{cc} - V_C}{R_C} = \frac{18 - 12}{4.7K} = 1.27\ mA$$

$$V_B = \frac{R_2}{R_1 + R_2} V_{cc} \quad \text{—①}$$

$$I_E R_E = V_B - V_{BE}$$

$$V_B = I_E R_E + V_{BE}$$

$$= 1.27m \times 1.2K + 0.7$$

$$V_B = 2.2\ V$$

① ⇒

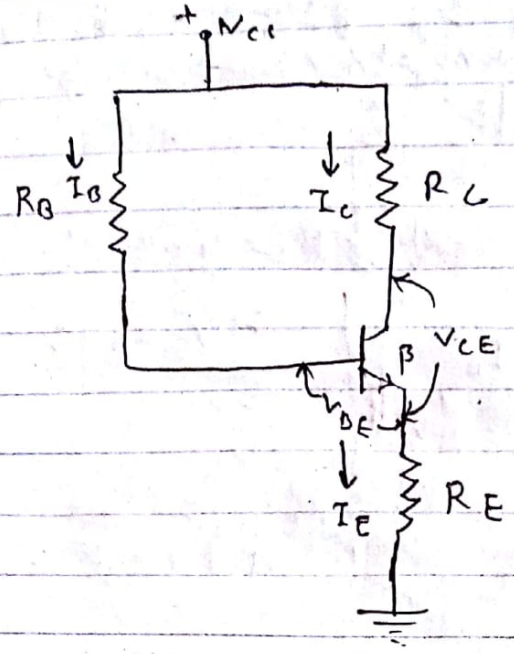
$$2.2 = \frac{5.6K}{R_1 + 5.6K} \times 18$$

$$2.2R_1 + 12.32K = 100.8K$$

$$R_1 = 40.2K$$

$$V_E = I_E R_E = 1.27m \times 1.2K = 1.52\ V$$

★ Emitter Stabilized Bias circuit :-



For a fixed bias ckt. R_E is added to improve the stability. Let us analys the ckt.

★ KVL to the base - Emitter loop

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE} - I_E R_E}{R_B} \quad \text{— (1)}$$

★ KVL to collector - Emitter loop

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C + I_E R_E$$

(1) $\Rightarrow$ $V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$

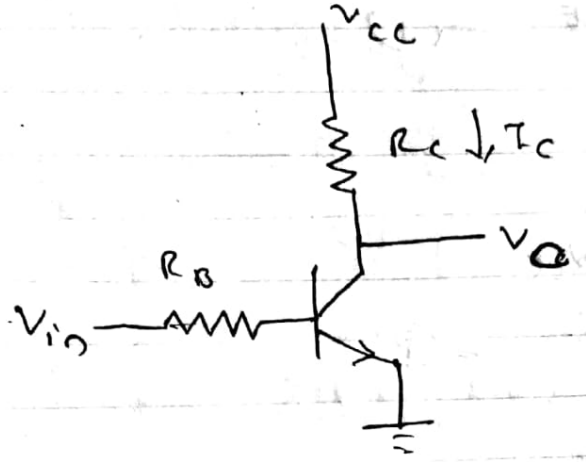
$$I_B [R_B + (\beta + 1) R_E] = V_{CC} - V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}}$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_E + R_C)}$$

$$\frac{V_{CC} - V_{BE}}{R_B + (R_B + R_E)\beta}$$

Transistor as a switch or Inverter



W.K.T. when trans. is biased such that its Q-point lies at centre of d.c. load line trans. acts as an amplifier. ~~////~~ when trans. is ~~acts~~ operated in cutoff & sat. region, its acts as switch.

These switching ckt. are used in computers & other control appl?.

Apply KVL to B-E

$V_{in} = I_B R_B + V_{BE}$

$I_B = \frac{V_{in} - V_{BE}}{R_B}$ — (1)

KVL to C-

$V_{CC} = I_C R_C + V_{CE}$

$I_C = \frac{V_{CC} - V_{CE}}{R_C}$ — (2)

here o/p vtg.

$V_C = V_{CE}$ — (3)

Let us Steady the foll^n cases.

case i) $V_{in} = V$

because of H.V. trans. turn ON, which produces heavy base current & make trans. to work in sat. region.

w.k.T. in Sat. region

$I_C = I_{C(sat)}$, $V_{CE} = V_{CE(sat)}$

(2) ⇒

$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$ — (4)

From (3)

$V_C = V_{CE(sat)}$ — (5)

before sat. trans. in active region i.e.

$I_{B(max)} = \frac{I_{C(sat)}}{\beta}$ — (6)

$\min I_{B(max)} > \frac{I_{C(sat)}}{\beta_{dc}}$ — (7)

To make trans. work in Sat. region the

$I_B > I_{B(max)}$

$I_B > \frac{I_{C(sat)}}{\beta_{dc}}$ — (7)

Tipical value of I_B for sat is 120% to 150% of $I_{B(max)}$. Here resistance bet' 'C' to 'E' is

$$R_{(sat)} = \frac{V_{c(sat)}}{I_{c(sat)}} \quad -(8)$$

for ideal

$$V_{CE} = 0$$

~~$R_{sat} = 0\,\Omega$~~

(4) $\Rightarrow$ $I_{c(sat)} = \frac{V_{cc}}{R_c}$

(5) $\Rightarrow$ $V_c = 0V$

(8) $\Rightarrow$ $R_{sat} = 0\,\Omega$

It means S.C. occurs bet' 'C' & 'E' terminal

Case ii)

$V_{in} = 0V$

$I_B = 0$

cut-OFF.

$I_c = I_{CEO}$

$V_{CE(cutoff)} = V_{cc} + I_{CEO} R_c$

$R_{cutoff} = \frac{V_{CE(cutoff)}}{I_{CEO}}$

$I_{CEO} \simeq 0$

$R_{cutoff} = \infty$

$V_{CE(cutoff)} = V_{cc}$