MODULE I

INTRODUCTION TO POWER ELECTRONICS:

Power Electronics is a field which combines Power (electric power), Electronics and Control systems.

Power engineering deals with the static and rotating power equipment for the generation, transmission and distribution of electric power.

Electronics deals with the study of solid state semiconductor power devices and circuits for Power conversion to meet the desired control objectives (to control the output voltage and output power).

Power electronics may be defined as the subject of applications of solid state power semiconductor devices (Thyristors) for the control and conversion of electric power.

Power electronics deals with the study and design of Thyristorised power controllers for variety of application like Heat control, Light/Illumination control, Motor control - AC/DC motor drives used in industries, High voltage power supplies, Vehicle propulsion systems, High voltage direct current (HVDC) transmission.

BRIEF HISTORY OF POWER ELECTRONICS

The first Power Electronic Device developed was the Mercury Arc Rectifier during the year 1900. Then the other Power devices like metal tank rectifier, grid controlled vacuum tube rectifier, ignitron, phanotron, thyratron and magnetic amplifier, were developed & used gradually for power control applications until 1950.

The first SCR (silicon controlled rectifier) or Thyristor was invented and developed by Bell Lab's in 1956 which was the first PNPN triggering transistor.

The second electronic revolution began in the year 1958 with the development of the commercial grade Thyristor by the General Electric Company (GE). Thus the new era of power electronics was born. After that many different types of power semiconductor devices & power conversion techniques have been introduced.The power electronics revolution is giving us the ability to convert, shape and control large amounts of power.

APPLICATIONS OF POWER ELECTRONICS

Advertising, air conditioning, aircraft power supplies, alarms, appliances - (domestic and industrial), audio amplifiers, battery chargers, blenders, blowers, boilers, burglar alarms, cement kiln, chemical processing, clothes dryers, computers, conveyors, cranes and hoists, dimmers (light dimmers), displays, electric door openers, electric dryers, electric fans, electric vehicles, electromagnets, electro mechanical electro plating, electronic ignition, electrostatic precipitators, elevators, fans, flashers, food mixers, food warmer trays, fork lift trucks, furnaces, games, garage door openers, gas turbine starting, generator exciters, grinders, hand power tools, heat controls, high frequency lighting, HVDC transmission, induction heating, laser power supplies, latching relays, light flashers, linear induction motor controls, locomotives, machine tools, magnetic recording, magnets, mass transit railway system, mercury arc lamp ballasts, mining, model trains, motor controls, motor drives, movie projectors, nuclear reactor control rod, oil well drilling, oven controls, paper mills, particle accelerators, phonographs, photo copiers, power suppliers, printing press, pumps and compressors, radar/sonar power supplies, refrigerators, regulators, RF amplifiers, security systems, servo systems, sewing

machines, solar power supplies, solid-state contactors, solid-state relays, static circuit breakers, static relays, steel mills, synchronous motor starting, TV circuits, temperature controls, timers and toys, traffic signal controls, trains, TV deflection circuits, ultrasonic generators, UPS, vacuum cleaners, VAR compensation, vending machines, VLF transmitters, voltage regulators, washing machines, welding equipment.

POWER ELECTRONIC APPLICATIONS

COMMERCIAL APPLICATIONS

Heating Systems Ventilating, Air Conditioners, Central Refrigeration, Lighting, Computers and Office equipments, Uninterruptible Power Supplies (UPS), Elevators, and Emergency Lamps.

DOMESTIC APPLICATIONS

Cooking Equipments, Lighting, Heating, Air Conditioners, Refrigerators & Freezers, Personal Computers, Entertainment Equipments, UPS.

INDUSTRIAL APPLICATIONS

Pumps, compressors, blowers and fans. Machine tools, arc furnaces, induction furnaces, lighting control circuits, industrial lasers, induction heating, welding equipments.

AEROSPACE APPLICATIONS

Space shuttle power supply systems, satellite power systems, aircraft power systems.

TELECOMMUNICATIONS

Battery chargers, power supplies (DC and UPS), mobile cell phone battery chargers.

TRANSPORTATION

Traction control of electric vehicles, battery chargers for electric vehicles, electric locomotives, street cars, trolley buses, automobile electronics including engine controls.

UTILITY SYSTEMS

High voltage DC transmission (HVDC), static VAR compensation (SVC), Alternative energy sources (wind, photovoltaic), fuel cells, energy storage systems, induced draft fans and boiler feed water pumps.

POWER SEMICONDUCTOR DEVICES

- Power Diodes.
- Power transistors (BJT's).
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Power MOSFETS.
IGBT's.
Thyristors

Thyristors are a family of p-n-p-n structured power semiconductor switching devices

SCR's (Silicon Controlled Rectifier)

The silicon controlled rectifier is the most commonly and widely used member of the thyristor family. The family of thyristor devices include SCR's, Diacs, Triacs, SCS, SUS, LASCR's and so on.

POWER SEMICONDUCTOR DEVICES USED IN POWER ELECTRONICS

The first thyristor or the SCR was developed in 1957. The conventional Thyristors (SCR's) were exclusively used for power control in industrial applications until 1970. After 1970, various types of power semiconductor devices were developed and became commercially available. The power semiconductor devices can be divided broadly into five types

- Power Diodes.
- Thyristors.
- Power BJT's.
- Power MOSFET's.
- Insulated Gate Bipolar Transistors (IGBT's).
- Static Induction Transistors (SIT's).

The Thyristors can be subdivided into different types

- Forced-commutated Thyristors (Inverter grade Thyristors)
- Line-commutated Thyristors (converter-grade Thyristors)
- Gate-turn off Thyristors (GTO).
- Reverse conducting Thyristors (RCT's).
- Static Induction Thyristors (SITH).
- Gate assisted turn-off Thyristors (GATT).
- Light activated silicon controlled rectifier (LASCR) or Photo SCR's.
- MOS-Controlled Thyristors (MCT's).

POWER DIODES

Power diodes are made of silicon p-n junction with two terminals, anode and cathode. P-N junction is formed by alloying, diffusion and epitaxial growth. Modern techniques in diffusion and epitaxial processes permit desired device characteristics.

The diodes have the following advantages

- High mechanical and thermal reliability
- High peak inverse voltage
- Low reverse current
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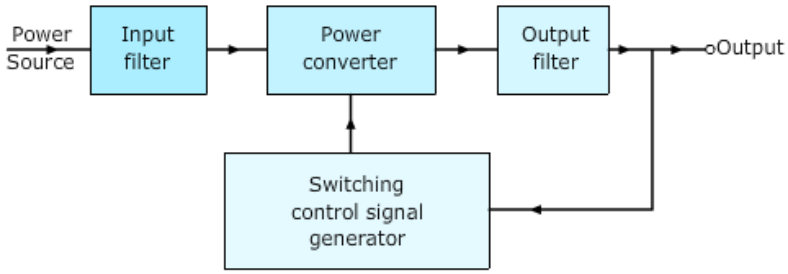
PERIPHERAL EFFECTS

The power converter operations are based mainly on the switching of power semiconductor devices. As a result due to the continuous & periodic repetitive turn-on and turn-off process of the switching devices used, the power converters introduce current and voltage harmonics (unwanted AC signal components) into the supply system and on the output of the converters.

These induced harmonics can cause problems of distortion of the output voltage, harmonic generation into the supply system, and interference with the communication and signaling circuits. It is normally necessary to introduce filters on the input side and output side of a power converter system so as to reduce the harmonic level to an acceptable magnitude. The figure below shows the block diagram of a generalized power converter with filters added. The application of power electronics to supply the sensitive electronic loads poses a challenge on the power quality issues and raises the problems and concerns to be resolved by the researchers. The input and output quantities of power converters could be either AC or DC. Factors such as total harmonic distortion (THD), displacement factor or harmonic factor (HF), and input power factor (IPF), are measures of the quality of the waveforms. To determine these factors it is required to find the harmonic content of the waveforms. To evaluate the performance of a converter, the input and output voltages/currents of a converter are expressed in Fourier series. The quality of a power converter is judged by the quality of its voltage and current waveforms.

Single Phase DC-AC Converter (Inverter) using MOSFETS

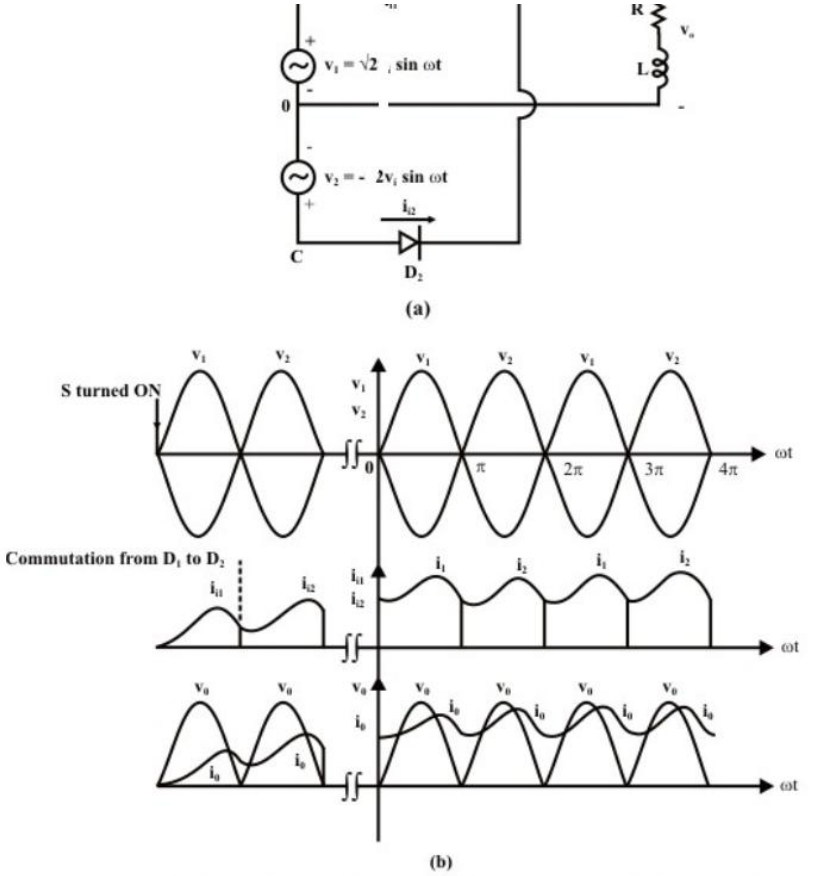


There are two types of full wave uncontrolled rectifiers commonly in use. If a split power supply is available (e.g. output from a split secondary transformer) only two diode will be required to produce a full wave rectifier. These are called split secondary rectifiers and are commonly used as the input stage of a linear dc voltage regulator. However, if no split supply is available the bridge configuration of the full wave rectifier is used. This is the more commonly used full wave uncontrolled rectifier configuration.

Full Wave Rectifier Circuit

The full wave rectifier circuit consists of two *power diodes* connected to a single load resistance (R_L) with each diode taking it in turn to supply current to the load. When point A of the transformer is positive with respect to point C, diode D_1 conducts in the forward direction as indicated by the arrows.

When point B is positive (in the negative half of the cycle) with respect to point C, diode D_2 conducts in the forward direction and the current flowing through resistor R is in the same direction for both half-cycles. As the output voltage across the resistor R is the phasor sum of the two waveforms combined, this type of full wave rectifier circuit is also known as a “bi-phase” circuit.



Split supply single phase uncontrolled full wave rectifier supplying an R - L load, (a) circuit diagram, (b) wave forms

When the switch is closed at the positive going zero crossing of v_1 the diode D_1 is forward biased and the load is connected to v_1. The currents i_0 and i_{i1} start rising through D_1. When v_1 reaches its negative going zero crossing both i_0 and i_{i1} are positive which keeps D_1 in conduction. Therefore, the voltage across D_2 is $v = v - v_1$. Beyond the negative going zero load voltage v_0 becomes equal to v_2 and D_1 starts blocking the voltage$v = v - v_2$. The current cycles.. It should be noted that the current i_0, once started, always remains positive. This mode of operation of the rectifier is called the "Continuous conduction mode" of operation.

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MODULE 2

POWER TRANSISTORS

Power transistors are devices that have controlled turn-on and turn-off characteristics. These devices are used a switching devices and are operated in the saturation region resulting in low on-state voltage drop. They are turned on when a current signal is given to base or control terminal. The transistor remains on so long as the control signal is present. The switching speed of modern transistors is much higher than that of thyristors and are used extensively in dc-dc and dc-ac converters. However their voltage and current ratings are lower than those of thyristors and are therefore used in low to medium power applications.

Power transistors are classified as follows

- Bipolar junction transistors(BJTs)
- Metal-oxide semiconductor filed-effect transistors(MOSFETs)
- Static Induction transistors(SITs)
- Insulated-gate bipolar transistors(IGBTs)

BIPOLAR JUNCTION TRANSISTORS

The need for a large blocking voltage in the off state and a high current carrying capability in the on state means that a power BJT must have substantially different structure than its small signal equivalent. The modified structure leads to significant differences in the I-V characteristics and switching behavior between power transistors and its logic level counterpart.

POWER TRANSISTOR STRUCTURE

If we recall the structure of conventional transistor we see a thin p-layer is sandwiched between two n-layers or vice versa to form a three terminal device with the terminals named as Emitter, Base and Collector.

The difference in the two structures is obvious.

A power transistor is a vertically oriented four layer structure of alternating p-type and n-type. The vertical structure is preferred because it maximizes the cross sectional area and through which the current in the device is flowing. This also minimizes on-state resistance and thus power dissipation in the transistor.

The doping of emitter layer and collector layer is quite large typically 10^{19} cm^{-3}. A special layer called the collector drift region (n^-) has a light doping level of 10^{14}.

The thickness of the drift region determines the breakdown voltage of the transistor. The base thickness is made as small as possible in order to have good amplification capabilities, however if the base thickness is small the breakdown voltage capability of the transistor is compromised.

Practical power transistors have their emitters and bases interleaved as narrow fingers as shown. The purpose of this arrangement is to reduce the effects of current crowding. This multiple emitter layout also reduces parasitic ohmic resistance in the base current path which reduces power dissipation in the transistor.

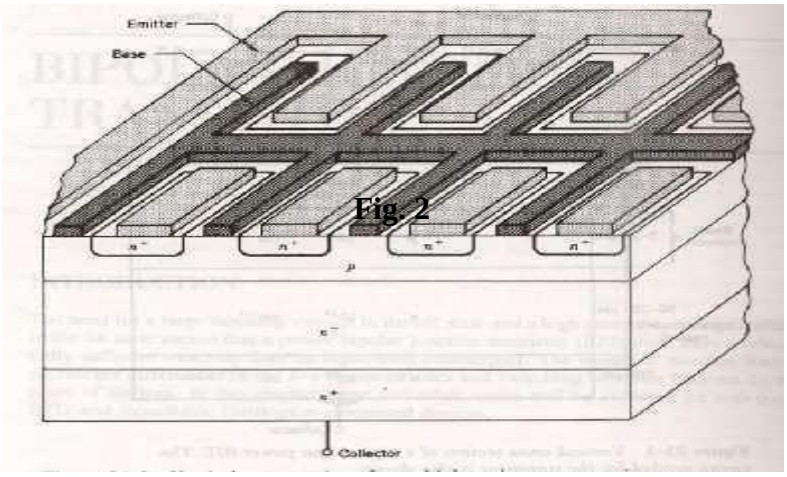


Fig. 2

STEADY STATE CHARACTERISTICS

Figure 3(a) shows the circuit to obtain the steady state characteristics. Fig 3(b) shows the input characteristics of the transistor which is a plot of I_B versus V_{BE} . Fig 3(c) shows the output characteristics of the transistor which is a plot I_C versus V_{CE} . The characteristics shown are that for a signal level transistor.

The power transistor has steady state characteristics almost similar to signal level transistors except that the V-I characteristics has a region of quasi saturation as shown by figure 4.

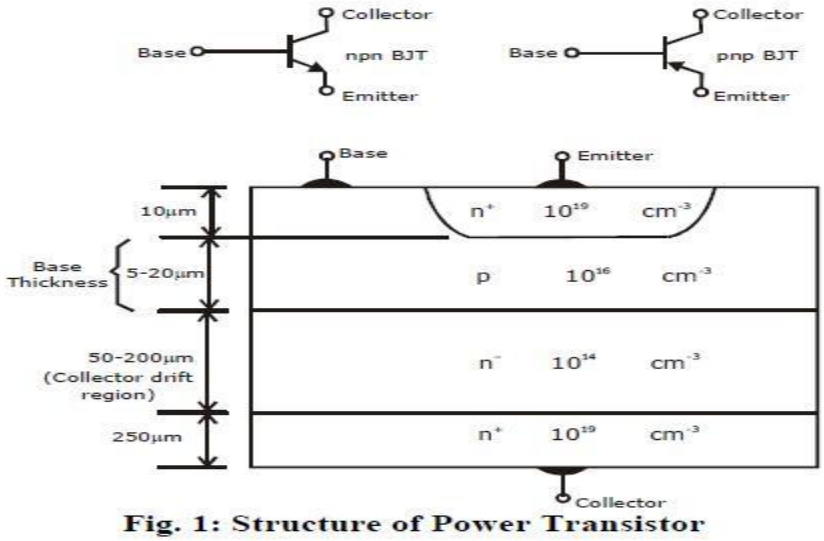
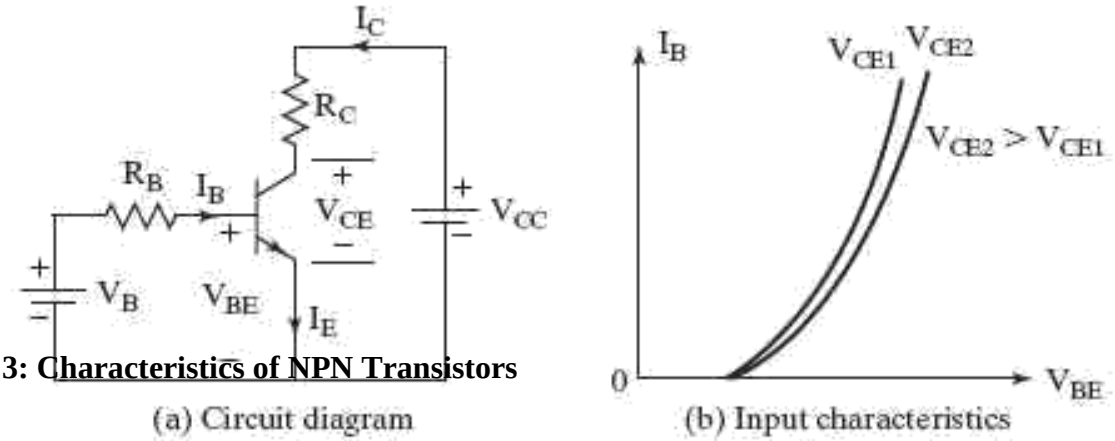


Fig. 1: Structure of Power Transistor



(a) Circuit diagram (b) Input characteristics

(c) Output characteristics

Fig. 3: Characteristics of NPN Transistors

There are four regions clearly shown: Cutoff region, Active region, quasi saturation and hard saturation. The cutoff region is the area where base current is almost zero. Hence no collector current flows and transistor is off. In the quasi saturation and hard saturation, the base drive is applied and transistor is said to be on. Hence collector current flows depending upon the load. The power BJT is never operated in the active region (i.e. as an amplifier) it is always operated between cutoff and saturation. The BV_{SUS} is the maximum collector to emitter voltage that can be sustained when BJT is carrying substantial collector current. The BV_{CEO} is the maximum collector to emitter breakdown voltage that can be sustained when base current is zero and BV_{CBO} is the collector base breakdown voltage when the emitter is open circuited

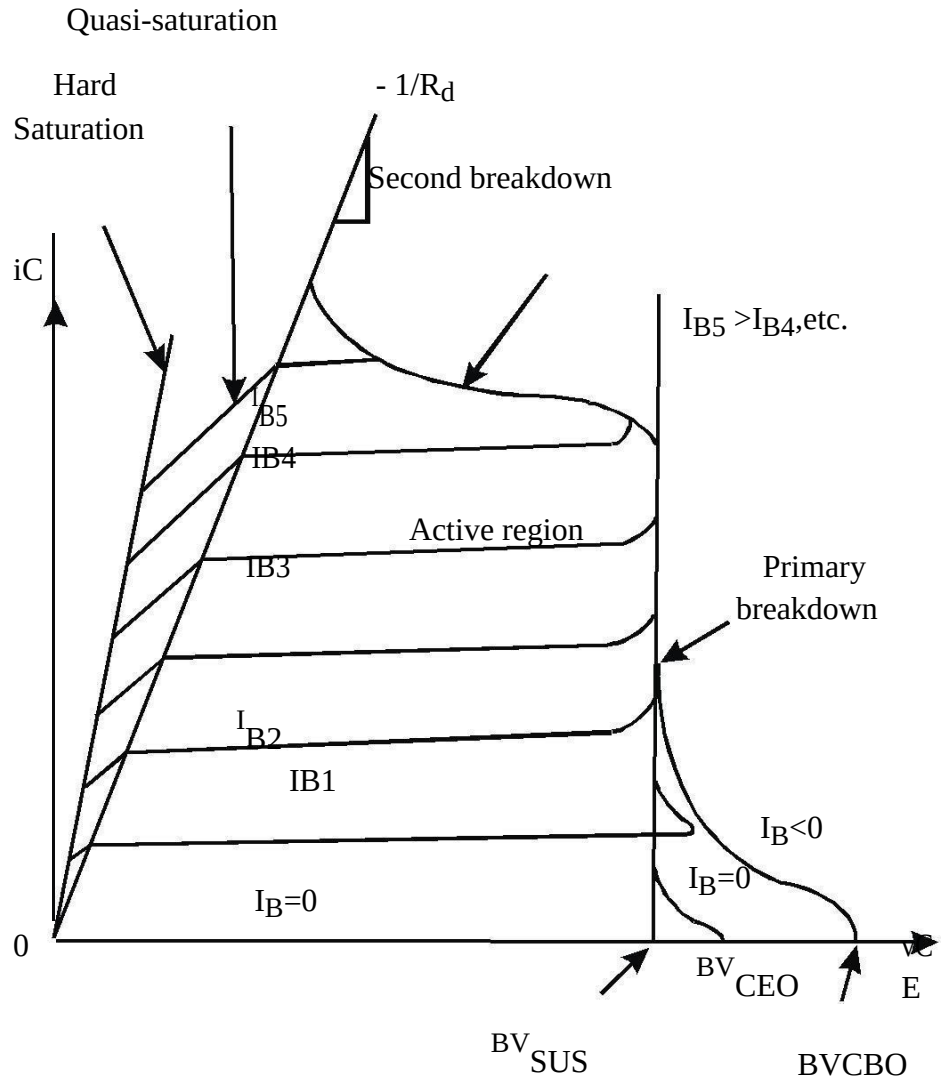


Fig. 4: Characteristics of NPN Power Transistors

The primary breakdown shown takes place because of avalanche breakdown of collector base junction. Large power dissipation normally leads to primary breakdown.

The second breakdown shown is due to localized thermal runaway. This is explained in detail later.

TRANSFER CHARACTERISTICS

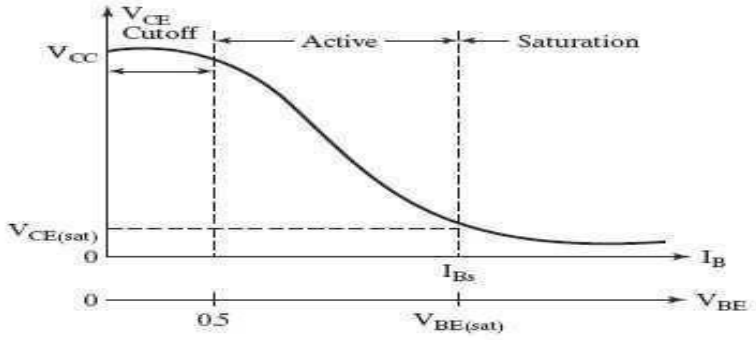


Fig. 5: Transfer Characteristics

TRANSISTOR AS A SWITCH

The transistor is used as a switch therefore it is used only between saturation and cutoff. From fig.5 we can write the following equations

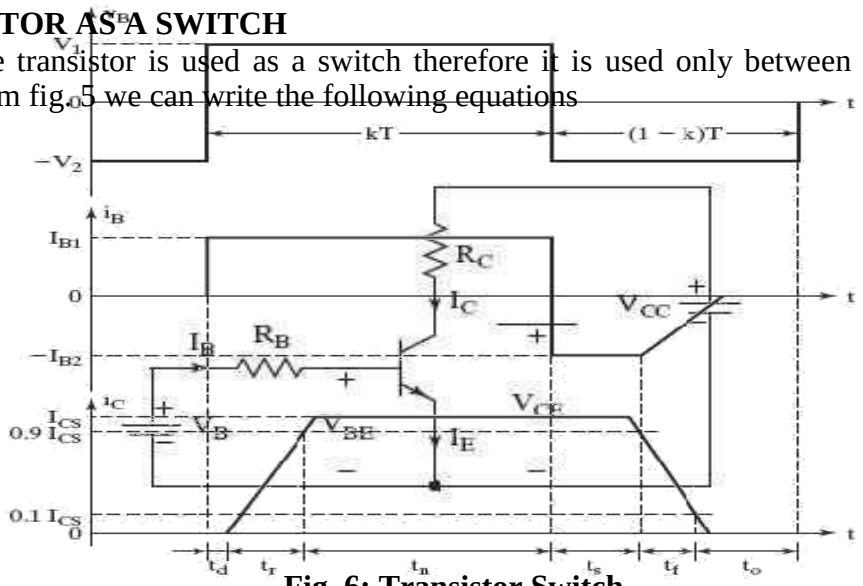


Fig. 6: Transistor Switch

If the base current is increased above I_{BM} ,V_{BE} increases, the collector current increases and V_{CE} falls belowV_{BE} . This continues until the CBJ is forward biased with V_{BC} of about 0.4 to 0.5V, the transistor than goes into saturation. The transistor saturation may be defined as the point above which any increase in the base current does not increase the collector current significantly.

In saturation, the collector current remains almost constant. If the collector emitter voltage is $V_{CE\,sat}$ the collector current is

V_{BE} increases due to increased base current resulting in increased power loss. Once the transistor is saturated, the CE voltage is not reduced in relation to increase in base current. However the power is increased at a high value of ODF, the transistor may be damaged due to thermal runaway. On the other hand if the transistor is under driven $I_B < I_{BS}$ it may operate in active region, V_{CE} increases resulting in increased power loss.

SWITCHING CHARACTERISTICS

A forward biased p-n junction exhibits two parallel capacitances; a depletion layer capacitance and a diffusion capacitance. On the other hand, a reverse biased p-n junction has only depletion capacitance. Under steady state the capacitances do not play any role. However under transient conditions, they influence turn-on and turn-off behavior of the transistor.

1.12 TRANSIENT MODEL OF BJT

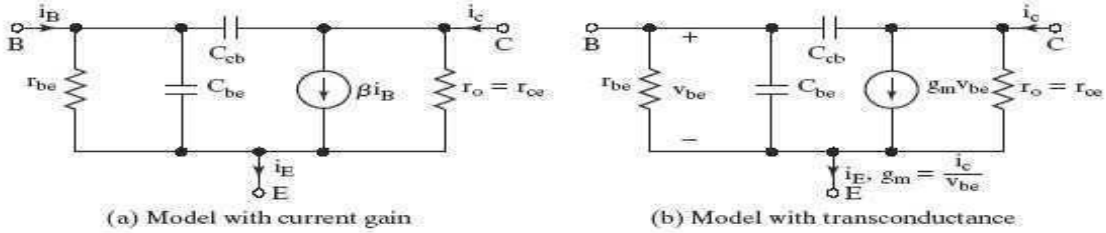


Fig. 7: Transient Model of BJT

Fig. 8: Switching Times of BJT

Due to internal capacitances, the transistor does not turn on instantly. As the voltage V_B rises from zero to V_1 and the base current rises to I_{B1}, the collector current does not respond immediately. There is a delay known as delay time td, before any collector current flows. The delay is due to the time required to charge up the BEJ to the forward bias voltage V_{BE}(0.7V). The collector current rises to the steady value of I_{CS} and this time is called rise time t_r.

The base current is normally more than that required to saturate the transistor. As a result excess minority carrier charge is stored in the base region. The higher the ODF, the greater is the amount of extra charge stored in the base. This extra charge which is called the saturating charge is proportional to the excess base drive.

This extra charge which is called the saturating charge, is proportional to the excess base drive and the corresponding current I_e.

When the input voltage is reversed from V_1 to $-V_2$, the reverse current $-I_{B2}$ helps to discharge the base. Without $-I_{B2}$ the saturating charge has to be removed entirely due to recombination and the storage time t_s would be longer.

Once the extra charge is removed, BEJ charges to the input voltage $-V_2$ and the base current falls to zero. t_f depends on the time constant which is determined by the reverse biased BEJ capacitance.

Turn-on time t_{on} : The turn-on time can be decreased by increasing the base drive for a fixed value of collector current. t_d is dependent on input capacitance does not change significantly with I_C . However t_r increases with increase in I_C .

Turn off time t_{off} : The storage time t_s is dependent on over drive factor and does not change significantly with I_C. t_f is a function of capacitance and increases with I_C. t_s & t_f can be reduced by providing negative base drive during turn-off. t_f is less sensitive to negative base drive.

Cross-over t_C : The crossover time t_C is defined as the interval during which the collector voltage V_{CE} rises from 10% of its peak off state value and collector current. I_C falls to 10% of its on-state value. t_C is a function of collector current negative base drive.

POWER DERATING

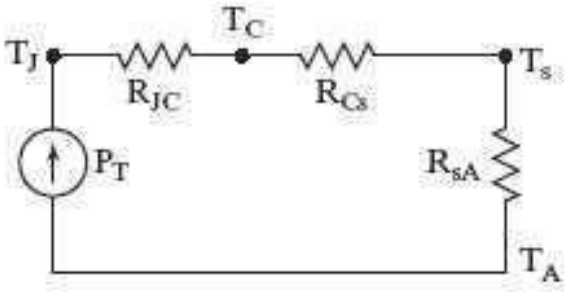


Fig. 11: Thermal Equivalent Circuit of Transistor

BREAK DOWN VOLTAGES

A break down voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted or biased in either forward or reverse direction.

BV_{SUS} : The maximum voltage between the collector and emitter that can be sustained across the transistor when it is carrying substantial collector current.

BV_{CEO} **:** The maximum voltage between the collector and emitter terminal with base open circuited.

BV_{CBO} **:** This is the collector to base break down voltage when emitter is open circuited.

BASE DRIVE CONTROL

This is required to optimize the base drive of transistor. Optimization is required to increase switching speeds. t_{on} can be reduced by allowing base current peaking during can be increased to a sufficiently high value to maintain the transistor in quasi-saturation region. t_{off} can be reduced by reversing base current and allowing base current peaking during turn off since increasing $I_{B\,2}$ decreases storage time.

A typical waveform for base current is shown.

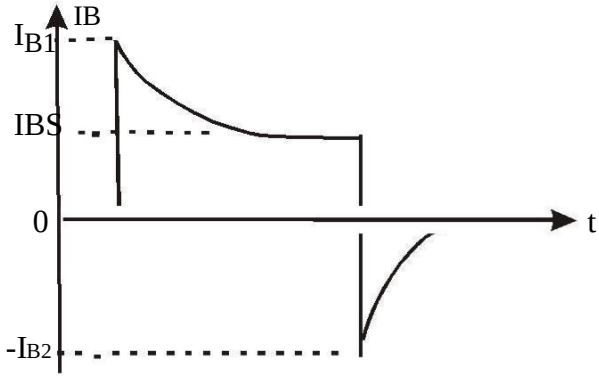


Fig. 12: Base Drive Current Waveform

Some common types of optimizing base drive of transistor are

- Turn-on Control.
- Turn-off Control.
- Proportional Base Control.
- Antisaturation Control

TURN-ON CONTROL

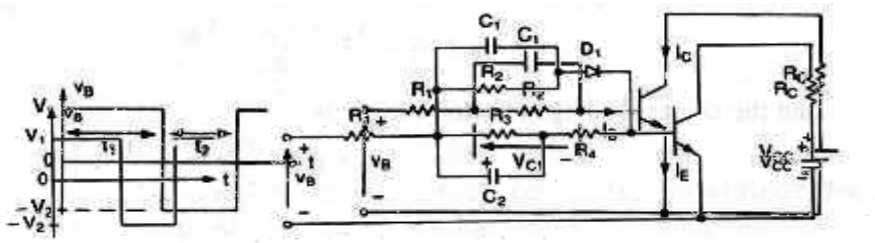


Fig. 13: Base current peaking during turn-on

When input voltage is turned on, the base current is limited by resistor R_1 and C_1 discharges through R_2. The discharging time constant is $_2 R_2 C_1$. To allow sufficient charging and discharging time, the width of base pulse must be $t_1 \square 5 \; |_1$ and off

TURN-OFF CONTROL

If the input voltage is changed to during turn-off the capacitor voltage V_C is added to V_2 as reverse voltage across the transistor. There will be base current peaking during turn off. As the capacitor C_1 discharges, the reverse voltage will be reduced to a steady state value, V_2 . If different turn-on and turn-off characteristics are required, a turn-off circuit using C_2 , R_3 & R_4 D_1 may be added. The diode isolates the forward base drive circuit from the reverse base drive circuit during turn off.

Fig: 14. Base current peaking during turn-on and turn-off

PROPORTIONAL BASE CONTROL

This type of control has advantages over the constant drive circuit. If the collector current changes due to change in load demand, the base drive current is changed in proportion to collector current.

When switch S_1 is turned on a pulse current of short duration would flow through the base of transistor Q_1 and Q_1 is turned on into saturation. Once the collector current starts to flow, a corresponding base current is induced due to transformer action. The transistor would latch on itself and S_1 can be turned off. For proper operation of the circuit, the magnetizing current which must be much smaller than the collector current should be as small as possible. The switch S_1 can be implemented by a small signal transistor and additional arrangement is necessary to discharge capacitor C_1 and reset the transformer core during turn-off of the power transistor.

ANTISATURATION CONTROL

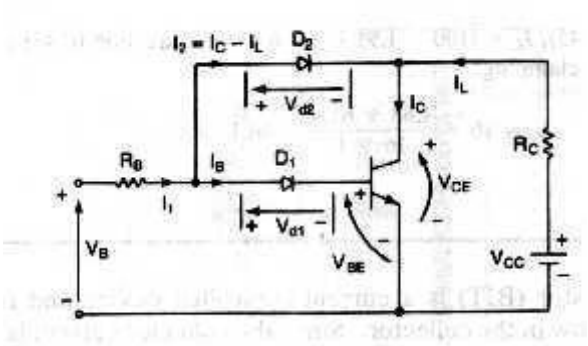


Fig: 16: Collector Clamping Circuit

If a transistor is driven hard, the storage time which is proportional to the base current increases and the switching speed is reduced. The storage time can be reduced by

operating the transistor in soft saturation rather than hard saturation. This can be accomplished by clamping CE voltage to a pre-determined level and the collector current is given by $I_C \approx \frac{VCC - VCM}{R_C}$.

Where V_{CM} is the clamping voltage and $V_{CM} \approx V_{CE\,sat}$.

This means that the CE voltage is raised above saturation level and there are no excess carriers in the base and storage time is reduced.

The clamping action thus results a reduced collector current and almost elimination of the storage time. At the same time, a fast turn-on is accomplished.

However, due to increased V_{CE}, the on-state power dissipation in the transistor is increased, whereas the switching power loss is decreased.

ADVANTAGES OF BJT'S

- BJT's have high switching frequencies since their turn-on and turn-off time are low.
- The turn-on losses of a BJT are small.
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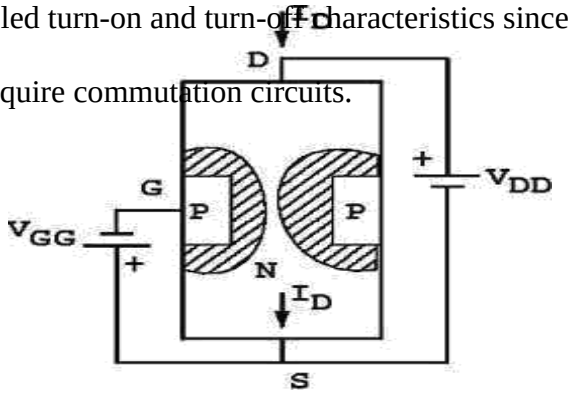
BJT has controlled turn-on and turn-off characteristics since base drive control is possible.

- BJT does not require commutation circuits.



DEMERITS OF BJT

- Drive circuit of BJT is complex.
- It has the problem of charge storage which sets a limit on switching frequencies. It cannot be used in parallel operation due to problems of negative temperature coefficient.

POWER MOSFETS

INTRODUCTION TO FET'S

FET's use field effect for their operation. FET is manufactured by diffusing two areas of p-type into the n-type semiconductor as shown. Each p-region is connected to a gate terminal; the gate is a p-region while source and drain are n-region. Since it is similar to two diodes one is a gate source diode and the other is a gate drain diode.

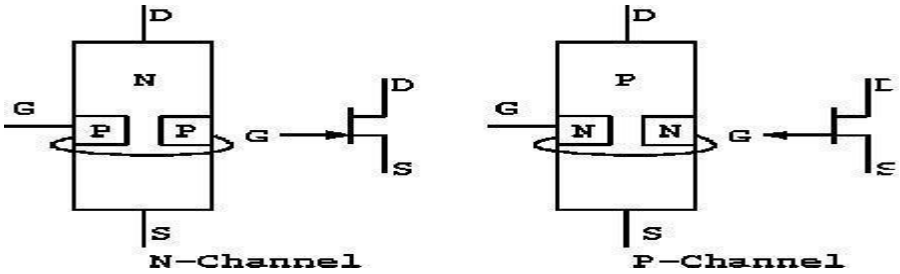


Fig:1: Schematic symbol of JFET

Fig. 2: Structure of FET with biasing

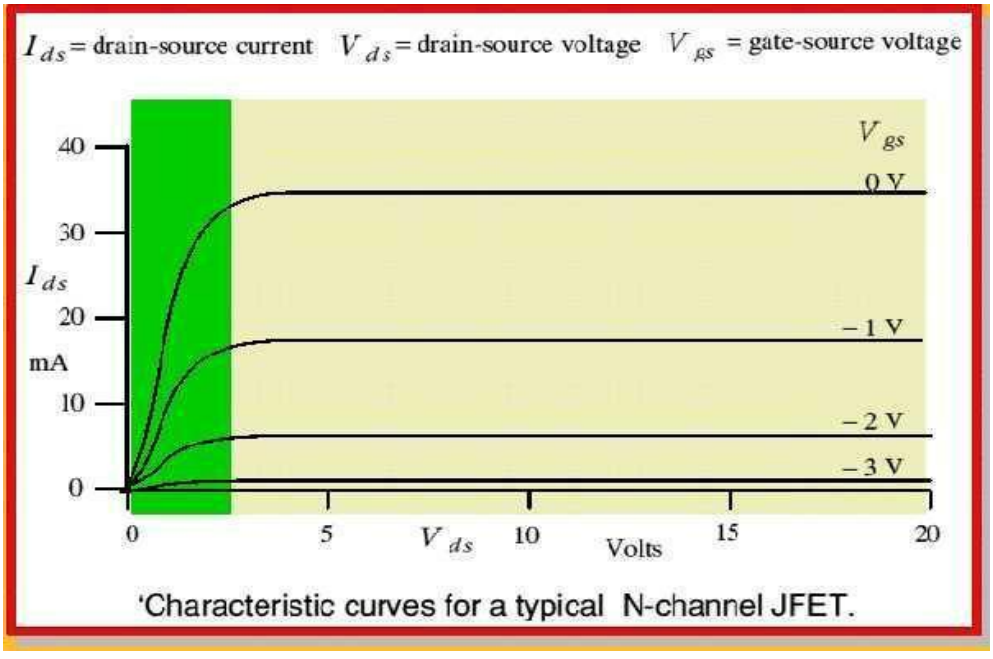
In BJT's we forward bias the B-E diode but in a JFET, we always reverse bias the gate-source diode. Since only a small reverse current can exist in the gate lead. Therefore $I_G \approx 0$, therefore $R_{in} \approx \infty ideal$.

The term field effect is related to the depletion layers around each p-region as shown. When the supply voltage V_{DD} is applied as shown it forces free electrons to flow from source to drain. With gate reverse biased, the electrons need to flow from source to drain, they must pass through the narrow channel between the two depletion layers. The more the negative gate voltage is the tighter the channel becomes.

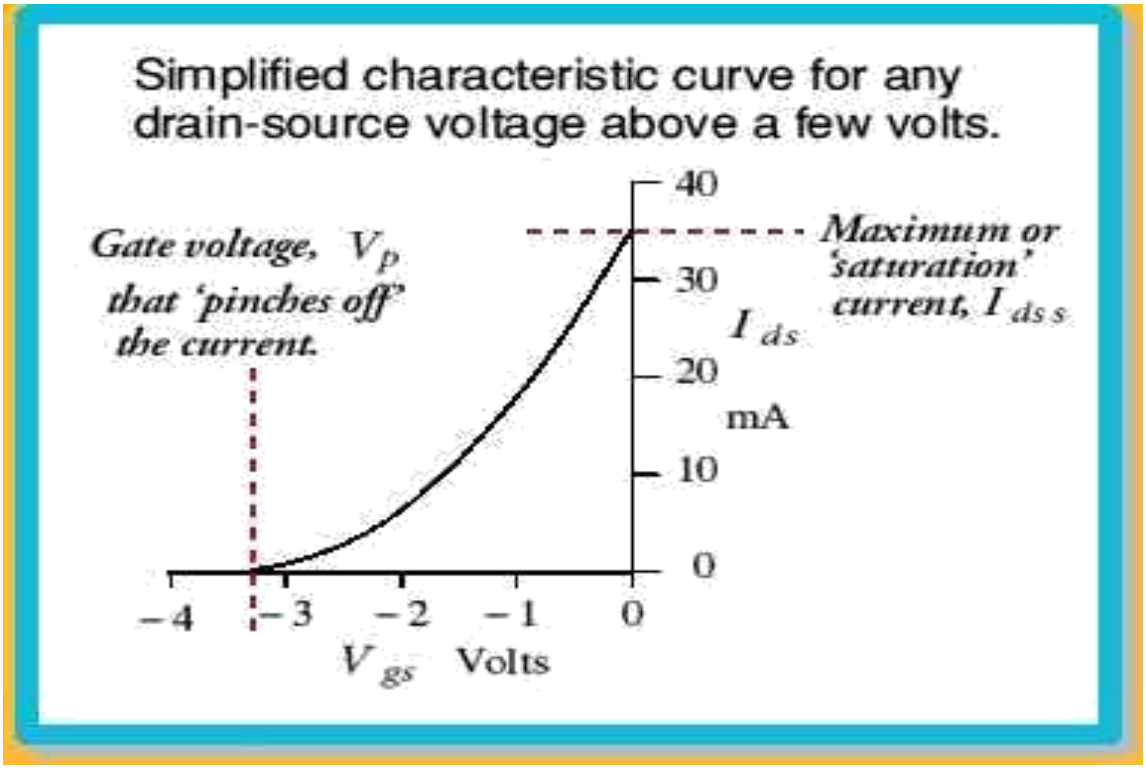
Therefore JFET acts as a voltage controlled device rather than a current controlled device.

JFET has almost infinite input impedance but the price paid for this is loss of control over the output current, since JFET is less sensitive to changes in the output voltage than a BJT.

JFET CHARACTERISTICS



'Characteristic curves for a typical N-channel JFET.



The maximum drain current out of a JFET occurs when V_{GS} V_{DS} is increased for 0 to a few volts, the current will increase as determined by ohms law. As V_{DS} approaches V_P the depletion region will widen, carrying a noticeable reduction in channel width. If V_{DS} is increased to a level where the two depletion region would touch a pinch-off will result. I_D now maintains a saturation level I_{DSS} . Between 0 volts and pinch off voltage V_P is the ohmic region. After V_P , the regions constant current or active
region.

If negative voltage is applied between gate and source the depletion region similar to those obtained with V_{GS} V_{DS} 0 are formed but at lower values of . Therefore saturation level is reached earlier.

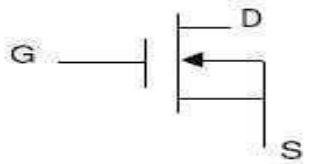
Classification of MOSFET

MOSFET stands for metal oxide semiconductor field effect transistor. There are two types of MOSFET

- Depletion type MOSFET
- Enhancement type MOSFET

DEPLETION TYPE MOSFET

CONSTRUCTION



Symbol of n-channel depletion type MOSFET

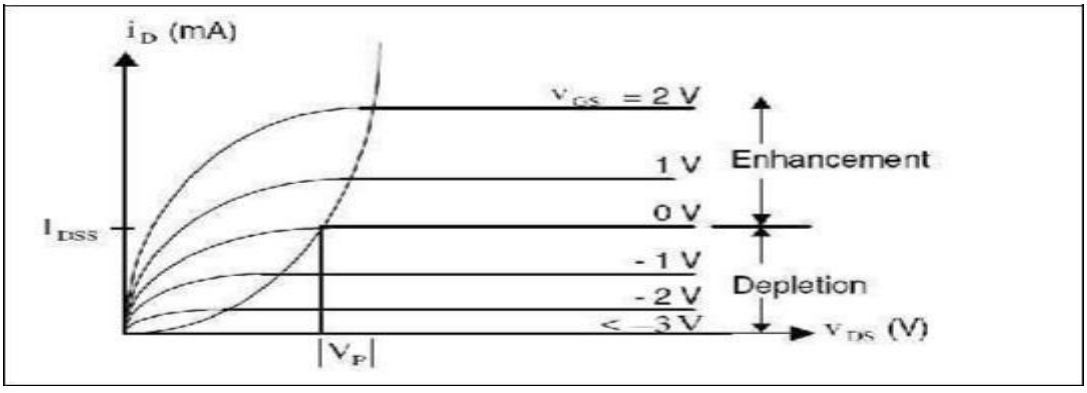
It consists of a highly doped p-type substrate into which two blocks of heavily doped n-type material are diffused to form a source and drain. A n-channel is formed by diffusing between source and drain. A thin layer of SiO_2 is grown over the entire surface and holes are cut in SiO_2 to make contact with n-type blocks. The gate is also connected to a metal contact surface but remains insulated from the n-channel by the SiO_2 layer. SiO_2 layer results in an extremely high input impedance of the order of 10^{10} to 10^{15} for this area.

OPERATION

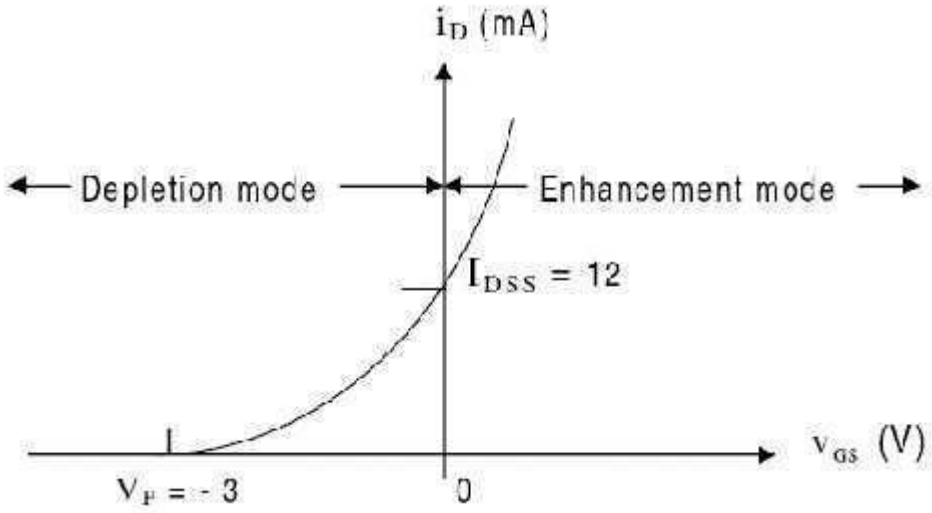
When V_{GS} $0V$ and V_{DS} is applied and current flows from drain to source similar to JFET. When V_{GS} $1V$, the negative potential will tend to pressure electrons towards the p-type substrate and attracts hole from p-type substrate. Therefore recombination occurs and will reduce the number of free electrons in the n-channel for conduction. Therefore with increased negative gate voltage I_D reduces.

For positive values, V_{gs}, additional electrons from p-substrate will flow into the channel and establish new carriers which will result in an increase in drain current with positive gate voltage.

DRAIN CHARACTERISTICS



TRANSFER CHARACTERISTICS



ENHANCEMENT TYPE MOSFET

Here current control in an n-channel device is now affected by positive gate to source voltage rather than the range of negative voltages of JFET's and depletion type MOSFET.

BASIC CONSTRUCTION

A slab of p-type material is formed and two n-regions are formed in the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions, but the absence of a channel between the doped n-regions. The SiO_2 layer is still present to isolate the gate metallic platform from the region between drain and source, but now it is separated by a section of p-type material.

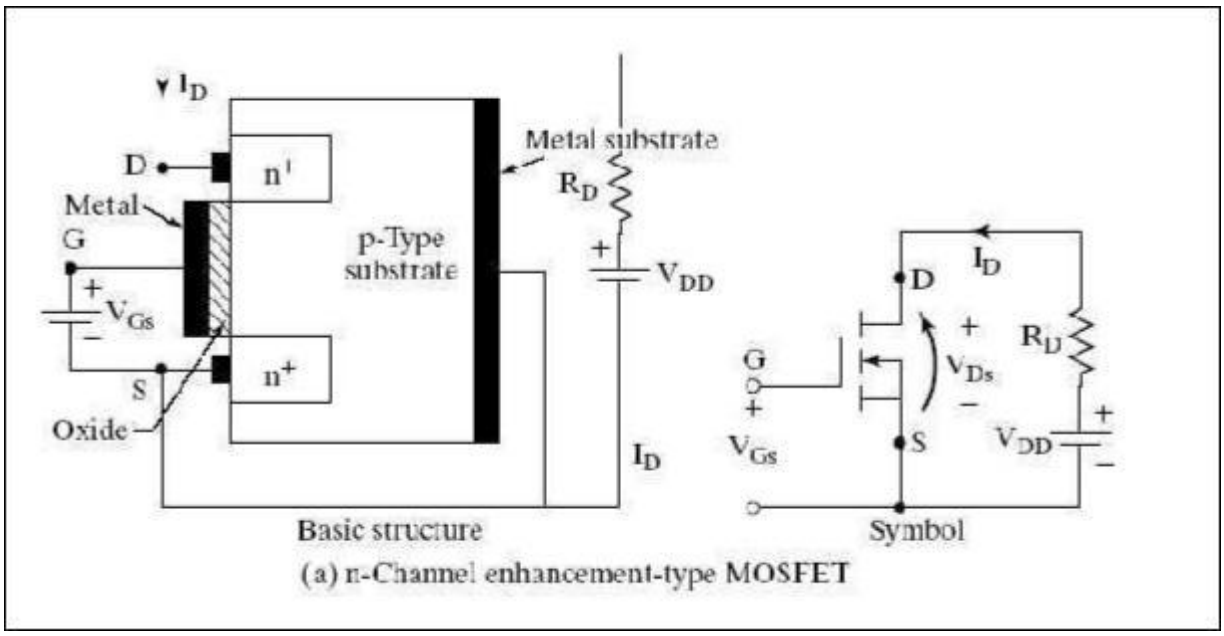


Fig. 5: Structure of n-channel enhancement type MOSFET

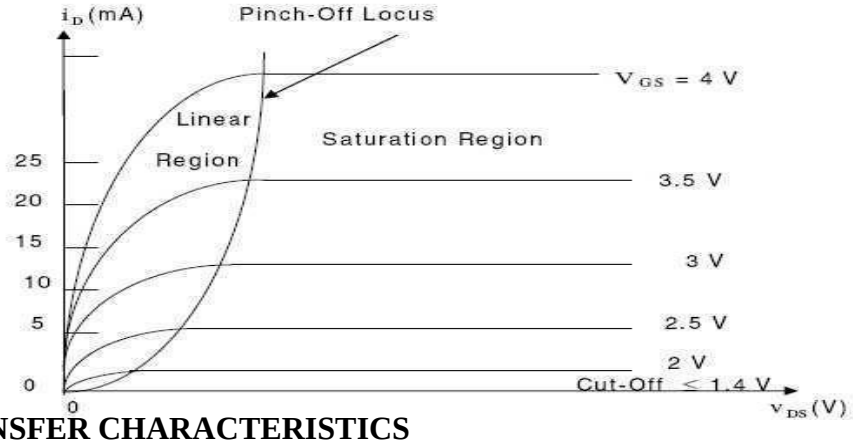
OPERATION

If V_{GS} $V0$ and a voltage is applied between the drain and source, the absence of a n-channel will result in a current of effectively zero amperes. With V_{DS} set at some positive voltage and V_{GS} set at 0V, there are two reverse biased p-n junction between the n-doped regions and p substrate to oppose any significant flow between drain and source.

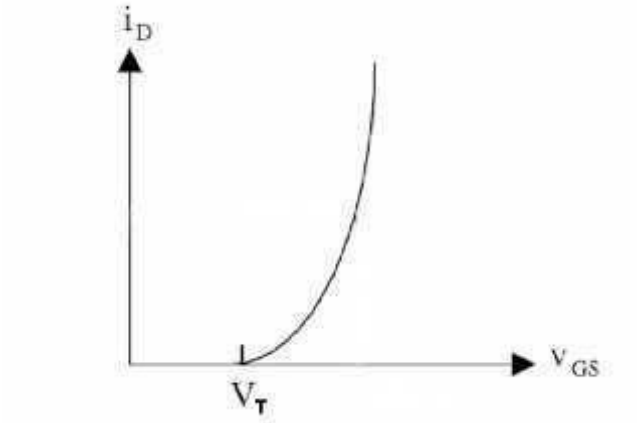
If both V_{DS} and V_{GS} have been set at some positive voltage, then positive potential at the gate will pressure the holes in the p-substrate along the edge of SiO_2 layer to leave the area and enter deeper region of p-substrate. However the electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The negative carriers will not be absorbed due to insulating SiO_2 layer, forming an inversion layer which results in current flow from drain to source.

The level of V_{GS} that results in significant increase in drain current is called threshold voltage V_T . As V_{GS} increases the density of free carriers will increase resulting in increased level of drain current. If V_{GS} is constant V_{DS} is increased; the drain current will eventually reach a saturation level as occurred in JFET.

DRAIN CHARACTERISTICS



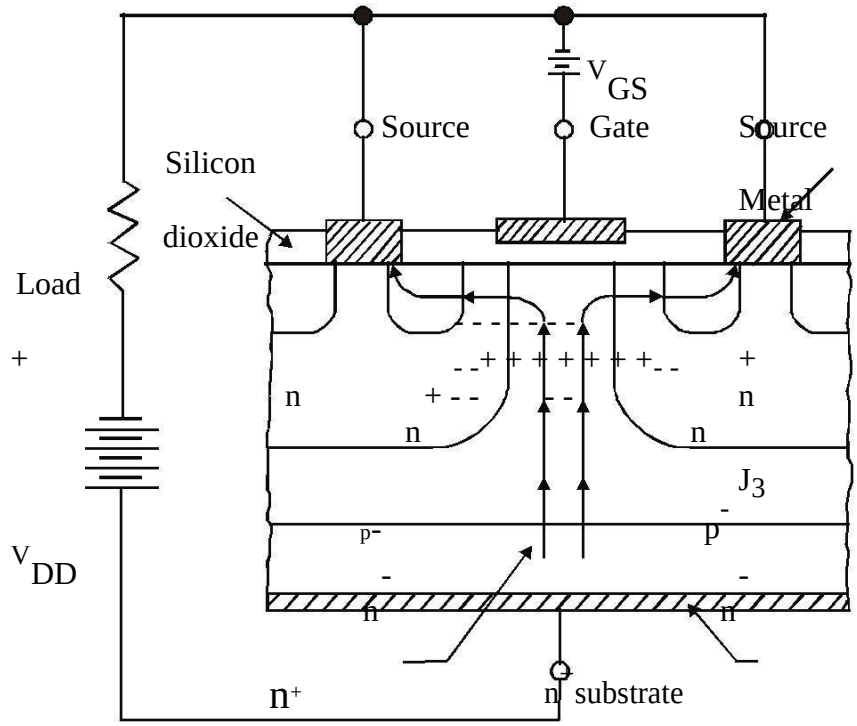
TRANSFER CHARACTERISTICS



POWER MOSFET'S

Power MOSFET's are generally of enhancement type only. This MOSFET is turned 'ON' when a voltage is applied between gate and source. The MOSFET can be turned 'OFF' by removing the gate to source voltage. Thus gate has control over the conduction of the MOSFET. The turn-on and turn-off times of MOSFET's are very small. Hence they operate at very high frequencies; hence MOSFET's are preferred in applications such as choppers and inverters. Since only voltage drive (gate-source) is required, the drive circuits of MOSFET are very simple. The paralleling of MOSFET's is easier due to their positive temperature coefficient. But MOSFTS's have high on-state resistance hence for higher currents; losses in the MOSFET's are substantially increased. Hence MOSFET's are used for low power applications.

CONSTRUCTION



Current path Metal layer

Drain

determines the voltage blocking capability of the device. On the other side of *n* substrate, a metal layer is deposited to form the drain terminal. Now *p* regions are diffused in the epitaxially grown *n* layer. Further *n* regions are diffused in the *p* regions as shown.

SiO_2 layer is added, which is then etched so as to fit metallic source and gate terminals.

A power MOSFET actually consists of a parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

When gate circuit voltage is zero and V_{DD} is present, *n p* junctions are reverse biased and no current flows from drain to source. When gate terminal is made positive with respect to source, an electric field is established and electrons from *n* channel in the *p* regions. Therefore a current from drain to source is established.

Power MOSFET conduction is due to majority carriers therefore time delays caused by removal of recombination of minority carriers is removed.

Because of the drift region the ON state drop of MOSFET increases. The thickness of the drift region determines the breakdown voltage of MOSFET. As seen a parasitic BJT is formed,

since emitter base is shorted to source it does not conduct.

SWITCHING CHARACTERISTICS

The switching model of MOSFET's is as shown in the figure 6(a). The various inter electrode capacitance of the MOSFET which cannot be ignored during high frequency switching are represented by C_{gs} , C_{gd} & C_{ds} . The switching waveforms are as shown in figure 7 . The turn on time t_d is the time that is required to charge the input capacitance to the threshold voltage level. The rise time t_r is the gate charging time from this threshold level to the full gate voltage V_{gsp} . The turn off delay time t_{doff} is the time required for the input capacitance to discharge from overdriving the voltage V_1 to the pinch off region. The fall time is the time required for the input capacitance to discharge from pinch off region to the threshold voltage. Thus basically switching ON and OFF depend on the charging time of the input gate capacitance.

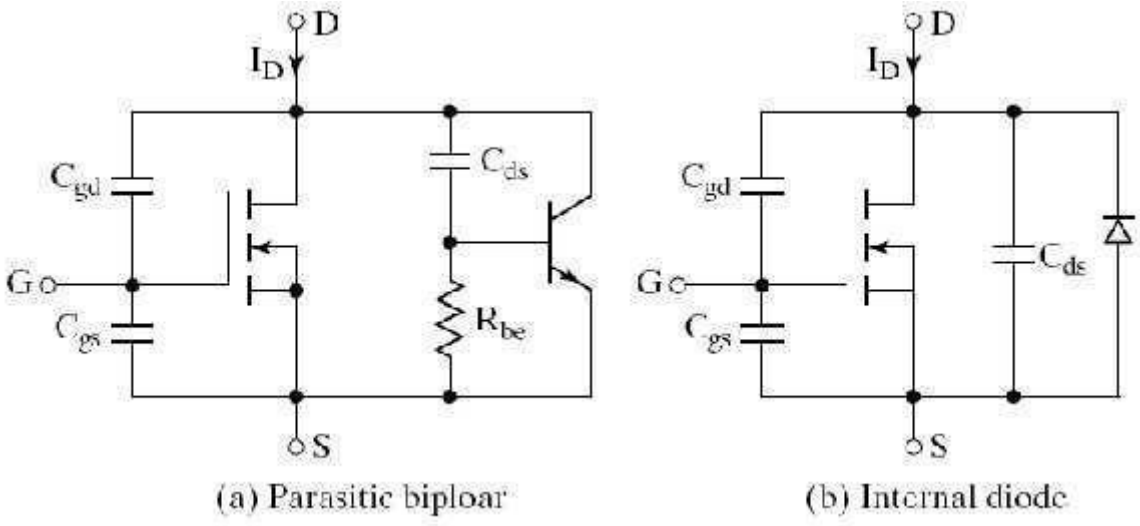
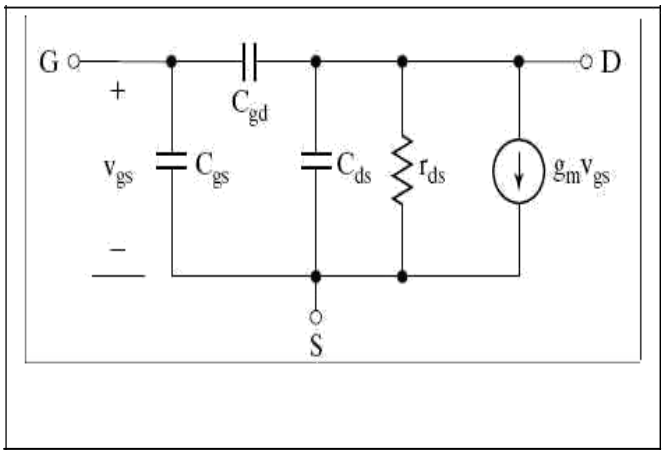


Fig.6: Switching model of MOSFET



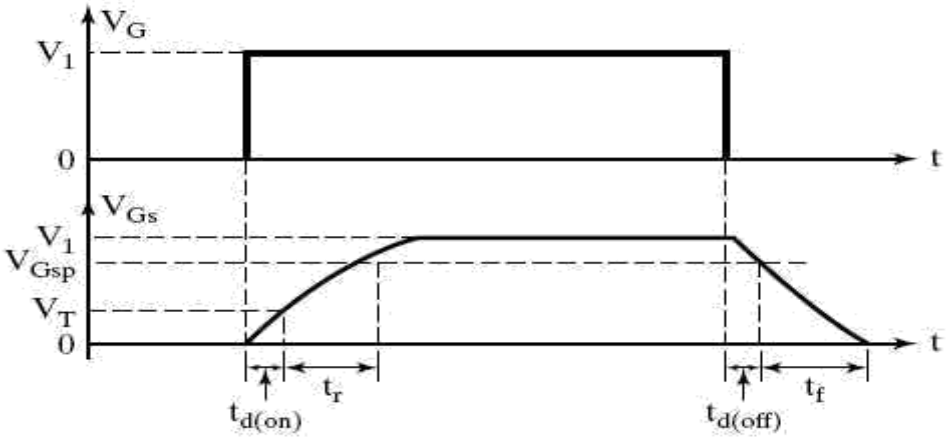


Fig.7: Switching waveforms and times of Power MOSFET

GATE DRIVE

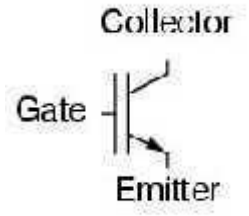
The turn-on time can be reduced by connecting a RC circuit as shown to charge the capacitance faster. When the gate voltage is turned on, the initial charging current of the capacitance is

Where R_S is the internal resistance of gate drive force.

COMPARISON OF MOSFET WITH BJT

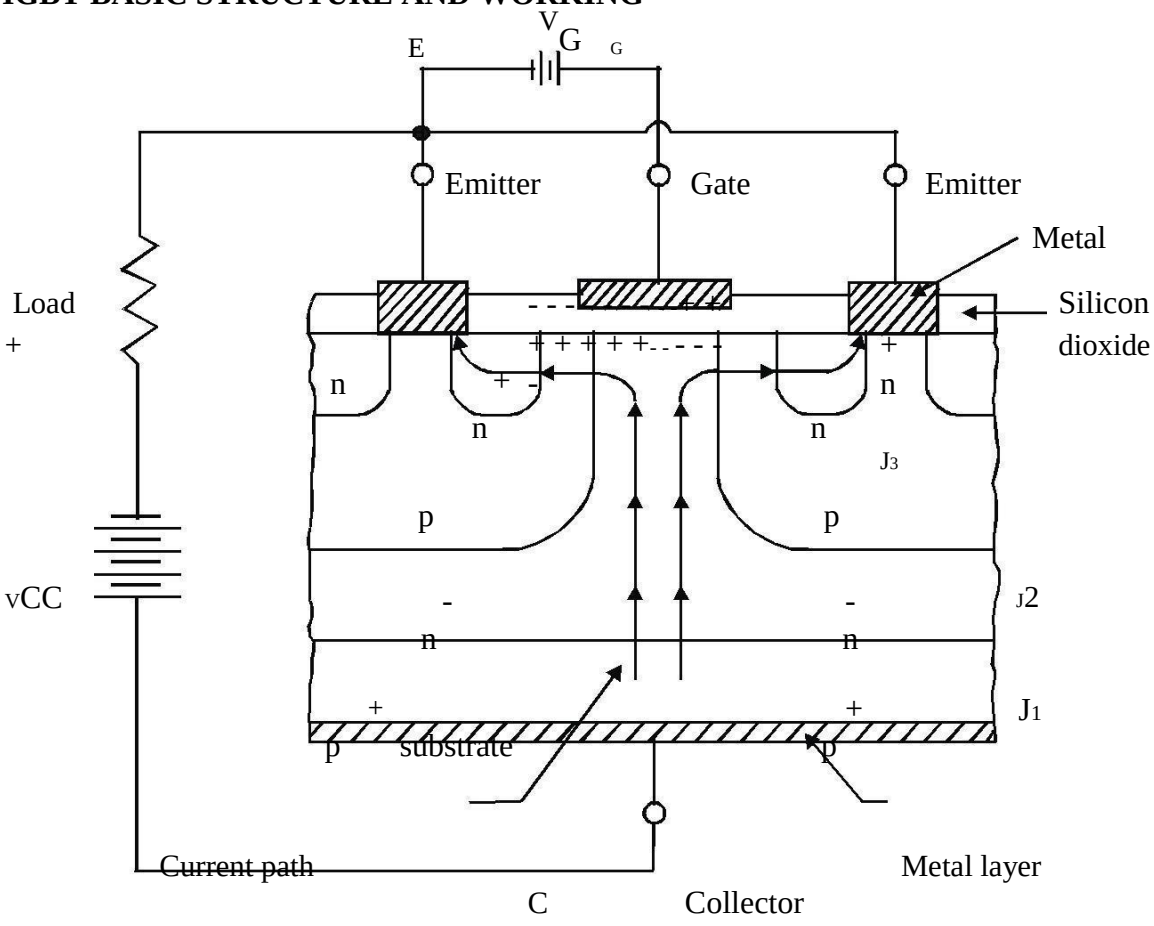
- Power MOSFETS have lower switching losses but its on-resistance and conduction losses are more. A BJT has higher switching loss bit lower conduction loss. So at high frequency applications power MOSFET is the obvious choice. But at lower operating frequencies BJT is superior.
- MOSFET has positive temperature coefficient for resistance. This makes parallel operation of MOSFET's easy. If a MOSFET shares increased current initially, it heats up faster, its resistance increases and this increased resistance causes this current to shift to other devices in parallel. A BJT is a negative temperature coefficient, so current shaving resistors are necessary during parallel operation of BJT's.
- In MOSFET secondary breakdown does not occur because it have positive temperature coefficient. But BJT exhibits negative temperature coefficient which results in secondary breakdown.
- Power MOSFET's in higher voltage ratings have more conduction losses.
  Power MOSFET's have lower ratings compared to BJT's . Power MOSFET's □
- 500V to 140A, BJT □ 1200V, 800A.

MOSIGT OR IGBT



The metal oxide semiconductor insulated gate transistor or IGBT combines the advantages of BJT's and MOSFET's.
Therefore an IGBT has high input impedance like a MOSFET and low-on state power loss as in a BJT. Further IGBT is free from second breakdown problem present in BJT.

IGBT BASIC STRUCTURE AND WORKING



It is constructed virtually in the same manner as a power MOSFET. However, the substrate is now a *p* layer called the collector.

When gate is positive with respect to positive with respect to emitter and with gate emitter voltage greater than V_{GSTH} , an n channel is formed as in case of power MOSFET. This *n* channel short circuits the *n* region with *n* emitter regions.

An electron movement in the *n* channel in turn causes substantial hole injection from *p* substrate layer into the epitaxially *n* layer. Eventually a forward current is established.

MOSFET is formed with input gate, emitter as source and *n* region as drain. Equivalent circuit is as shown below.

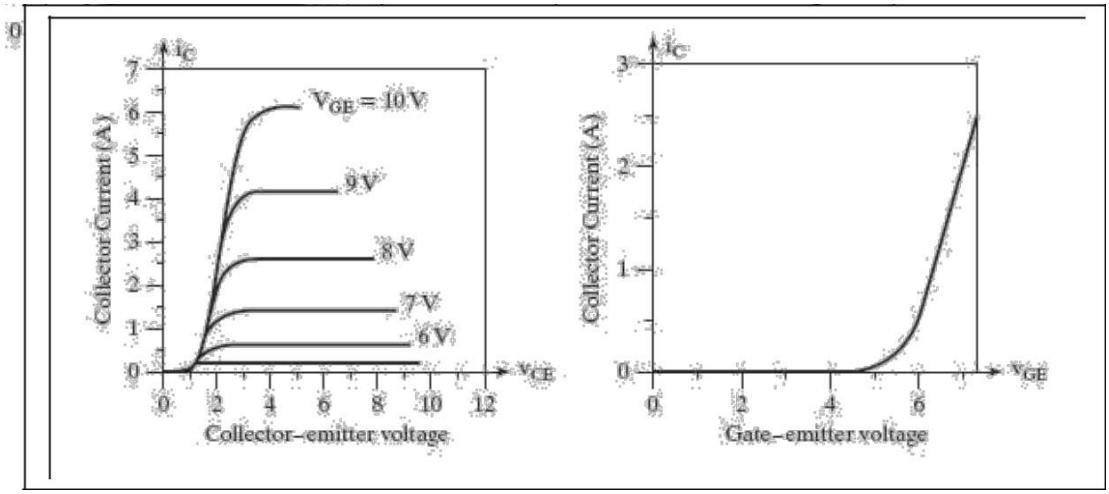
Also *p* serves as collector for pnp device and also as base for npn transistor. The two pnp and npn is formed as shown.

When gate is applied $V_{GS} \geq V_{GSth}$ MOSFET turns on. This gives the base drive to T_1 . Therefore T_1 starts conducting. The collector of T_1 is base of T_2 . Therefore regenerative action takes place and large number of carriers are injected into the *n* drift region. This reduces the ON-state loss of IGBT just like BJT.

When gate drive is removed IGBT is turn-off. When gate is removed the induced channel will vanish and internal MOSFET will turn-off. Therefore T_1 will turn-off it T_2 turns off.

Structure of IGBT is such that R_1 is very small. If R_1 small T_1 will not conduct therefore IGBT's are different from MOSFET's since resistance of drift region reduces when gate drive is applied due to *p* injecting region. Therefore ON state IGBT is very small.

IGBT CHARACTERISTICS



STATIC CHARACTERISTICS

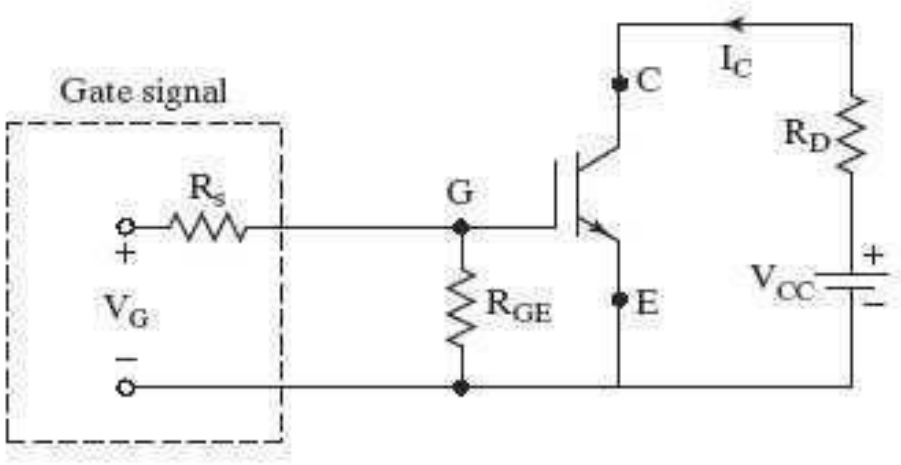


Fig. 9: IGBT bias circuit

Static V-I characteristics (I_C versus V_{CE})

Same as in BJT except control is by V_{GE} . Therefore IGBT is a voltage controlled device.

Transfer Characteristics (I_C versus V_{GE})

Identical to that of MOSFET. When V_{GE} □V_{GET} , IGBT is in off-state.

APPLICATIONS

Widely used in medium power applications such as DC and AC motor drives, UPS systems, Power supplies for solenoids, relays and contractors.

Though IGBT's are more expensive than BJT's, they have lower gate drive requirements, lower switching losses. The ratings up to 1200V, 500A.

SERIES AND PARALLEL OPERATION

Transistors may be operated in series to increase their voltage handling capability. It is very important that the series-connected transistors are turned on and off simultaneously. Other wise, the slowest device at turn-on and the fastest devices at turn-off will be subjected to the full voltage of the collector emitter circuit and the particular device may be destroyed due to high voltage. The devices should be matched for gain, transconductance, threshold voltage, on state voltage, turn-on time, and turn-off time. Even the gate or base drive characteristics should be identical.

Transistors are connected in parallel if one device cannot handle the load current demand. For equal current sharings, the transistors should be matched for gain, transconductance, saturation voltage, and turn-on time and turn-off time. But in practice, it is not always possible to meet these requirements. A reasonable amount of current sharing (45 to 55% with two transistors) can be obtained by connecting resistors in series with the emitter terminals as shown in the figure 10.

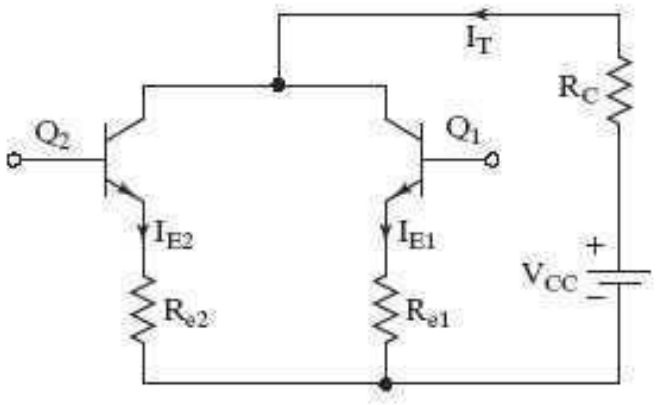


Fig. 10: Parallel connection of Transistors

The resistor will help current sharing under steady state conditions. Current sharing under dynamic conditions can be accomplished by connecting coupled inductors. If the current through Q_1 rises, the $l\, di/dt$ across L_1 increases, and a corresponding voltage of opposite polarity is induced across inductor L_2 . The result is low impedance path, and the current is shifted to Q_2 . The inductors would generate voltage spikes and they may be expensive and bulky, especially at high currents.

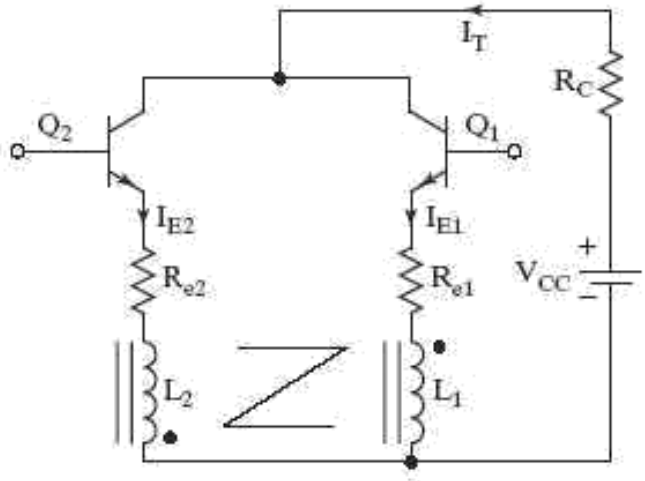
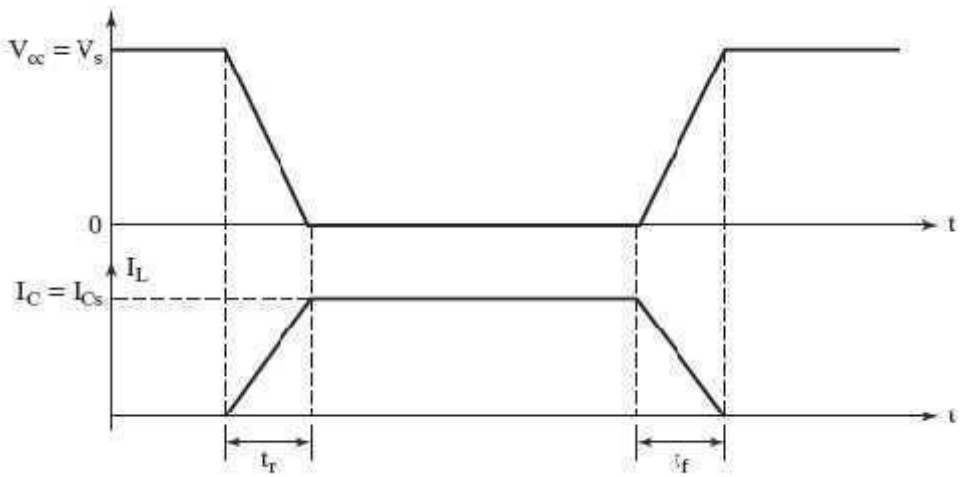


Fig. 11: Dynamic current sharing

BJTs have a negative temperature coefficient. During current sharing, if one BJT carries more current, its on-state resistance decreases and its current increases further, whereas MOSFETS have positive temperature coefficient and parallel operation is relatively easy. The MOSFET that initially draws higher current heats up faster and its on-state resistance increases, resulting in current shifting to the other devices. IGBTs require special care to match the characteristics due to the variations of the temperature coefficients with the collector current.

di/dt AND dv/dt LIMITATIONS

Transistors require certain turn-on and turn-off times. Neglecting the delay time t_d and the storage time t_s , the typical voltage and current waveforms of a BJT switch is shown below.



During turn-on, the collector rise and the di/dt is

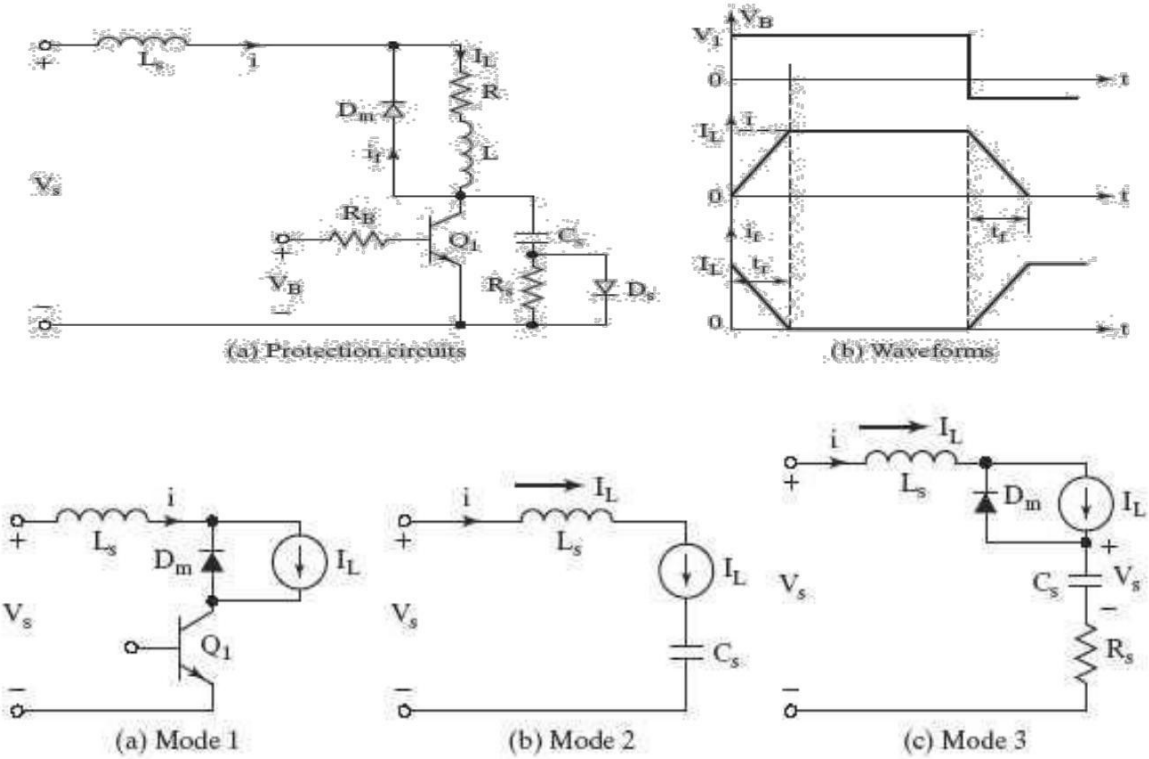
$$\frac{di}{dt} \square \frac{I}{L} \square \frac{I_{cs}}{t_r} \quad ...(1)$$

During turn off, the collector emitter voltage must rise in relation to the fall of the collector current, and is

$$\frac{dv}{dt} \square \frac{V_S}{t_f} \square \frac{V_{cc}}{t_f} \quad ...(2)$$

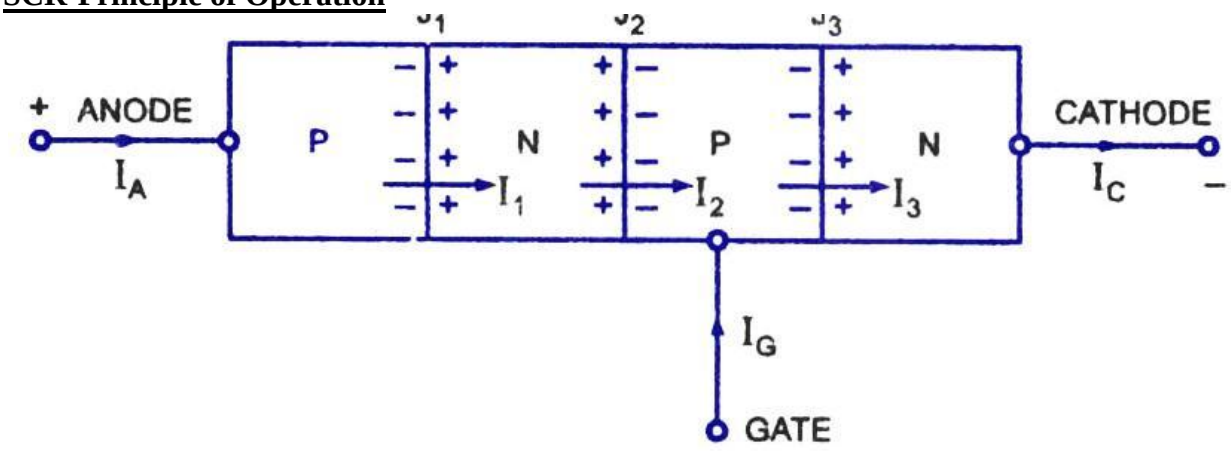
The conditions di/dt and dv/dt in equation (1) and (2) are set by the transistor switching characteristics and must be satisfied during turn on and turn off. Protection circuits are normally required to keep the operating di/dt and dv/dt within the allowable *limits of transistor. A typical switch with* di/dt and dv/dt protection is shown in figure *(a), with operating wave forms in figure (b). The RC network across the transistor is known as the snubber circuit or snubber and limits the* dv/dt . The inductor L_S , which *limits the* di/dt , is sometimes called series snubber.

Let us assume that under steady state conditions the load current I_L is free wheeling through diode D_m , which has negligible reverse reco`very time. When transistor Q_1 is turned on, the collector current rises and current of diode D_m falls, because D_m will behave as short circuited. The equivalent circuit during turn on is shown in figure below



MODULE 3

SCR-Principle of Operation



Diagrammatic Representation Showing Current Flow and Voltage Bias in An SCR

The **SCR** is a four-layer, three-junction and a three-terminal device and is shown in fig.a. The end P-region is the anode, the end N-region is the cathode and the inner P-region is the gate. The anode to cathode is connected in series with the load circuit. Essentially the device is a switch. Ideally it remains off (voltage blocking state), or appears to have an infinite impedance until both the anode and gate terminals have suitable positive voltages with respect to the cathode terminal.

The thyristor then switches on and current flows and continues to conduct without further gate signals. Ideally the thyristor has zero impedance in conduction state. For switching off or reverting to the blocking state, there must be no gate signal and the anode current must be reduced to zero. Current can flow only in one direction.

In absence of external bias voltages, the majority carrier in each layer diffuses until there is a built-in voltage that retards further diffusion. Some majority carriers have enough energy to cross the barrier caused by the retarding electric field at each junction. These carriers then become minority carriers and can recombine with majority carriers. Minority carriers in each layer can be accelerated across each junction by the fixed field, but because of absence of external circuit in this case the sum of majority and minority carrier currents must be zero.

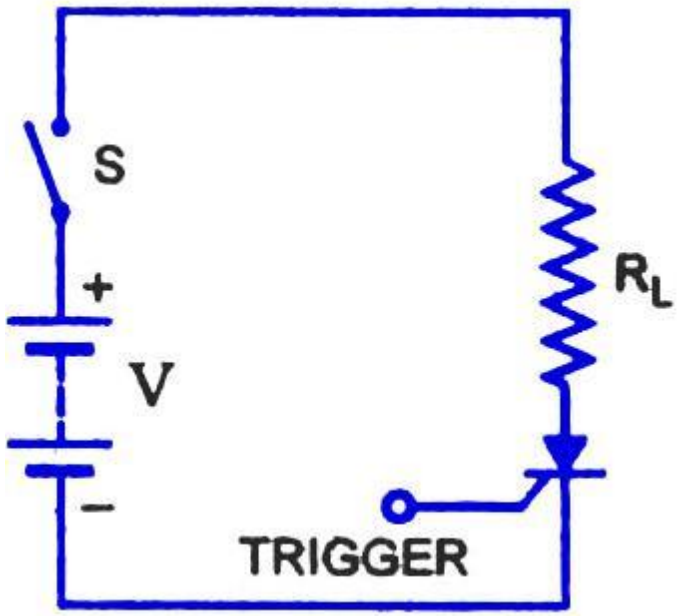
A voltage bias, as shown in figure, and an external circuit to carry current allow internal currents which include the following terms:

The current I_x is due to

- Majority carriers (holes) crossing junction J_1
- Minority carriers crossing junction J_1
- Holes injected at junction J_2 diffusing through the N-region and crossing junction J_1 and

- Minority carriers from junction J_2 diffusing through the N-region and crossing junction J_1. Similarly I_2 is due to six terms and I_3 is due to four terms.

Turning-off Methods of an SCR



As already mentioned in previous blog post, once the **SCR is fired**, it remains on even when triggering pulse is removed. This ability of the SCR to remain on even when gate current is removed is referred to as latching. So SCR cannot be turned off by simply removing the gate pulse.

There are three methods of switching off the **SCR, namely** natural commutation, reverse bias turn-off, and gate turn-off.

a) Natural Commutation

When the anode current is reduced below the level of the holding current, the SCR turns off. However, it must be noted that rated anode current is usually larger than 1,000 times the holding value. Since the anode voltage remains positive with respect to the cathode in a dc circuit, the anode current can only be reduced by opening the line switch S, increasing the load impedance R_L or shunting part of the load current through a circuit parallel to the SCR, i.e. short-circuiting the device.

(b) Reverse-bias Turn-off

A reverse anode to cathode voltage (the cathode is positive with respect to the anode) will tend to interrupt the anode current. The voltage reverses every half cycle in an ac circuit, so that an SCR in the line would be reverse biased every negative cycle and would turn off. This is called phase commutation or ac line commutation. To create a reverse biased voltage across the SCR, which is in the line of a dc circuit, capacitors can be used. The method of discharging a capacitor in parallel with an SCR to turn-off the SCR is called forced commutation.

In power electronic applications one advantage of using SCRs is that they are compact. The control equipment is also compact if integrated circuits are used. There has also been an attempt to miniaturize capacitors used for forced commutation and for filtering. The former use is important because the currents can be high and thermal dissipation takes high priority in design

considerations. Small sizes of capacitors are at present being achieved by the use of metalized plastic film or a plastic film and aluminium foil.

(c) Gate Turn Off

In some specially designed SCRs the characteristics are such that a negative gate current increases the holding current so that it exceeds the load current and the device turns-off. The current ratings are presently below 10 A and this type will not be considered further.

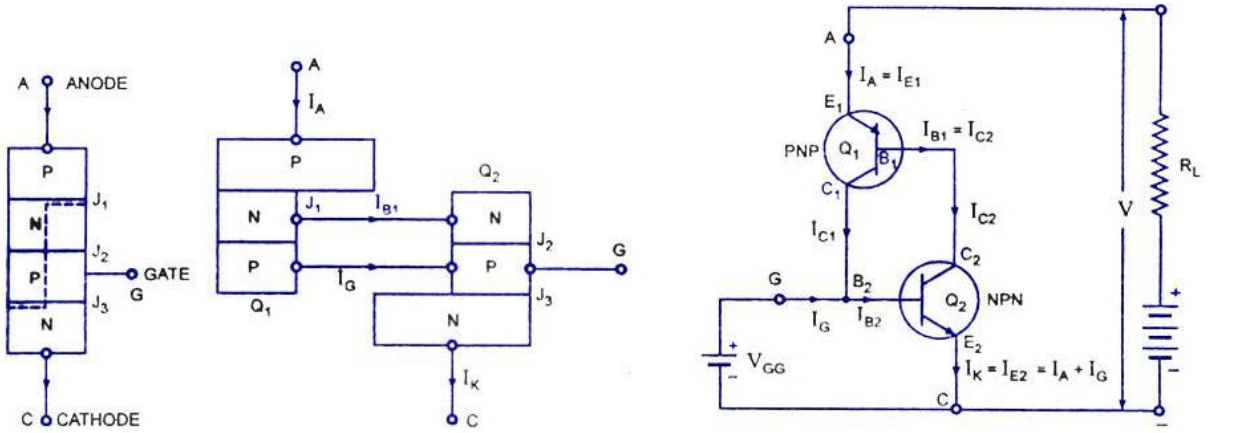
Two Transistor analogy of SCR

The principle of thyristor operation can be explained with the use of its two-transistor model (or two-transistor analogy). Fig. 4.15 (a) shows schematic diagram of a thyristor. From this figure, two-transistor model is obtained by bisecting the two middle layers, along the dotted line, in two separate halves as shown in Fig. 4.15 (b). In this figure, junctions J1 – j2and J2 -J3 can be considered to constitute pnp and npn transistors separately. The circuit representation of the two-transistor model of a thyristor is shown in Fig. 4.15 (c).

In the off-state of a transistor, collector current Ic is related to emitter current IE as

$I_C = \alpha I_E + I_{CBO}$

where α is the common-base current gain and I_{CB0} is the common-base leakage current of collector-base junction of a transistor.



SCR Split-up into Two Transistors *Two Transistor Equivalent Circuit of An SCR*

Two Transistor Model of An SCR

For transistor Q_1 in Fig. 4.15 (c), emitter current I_E = anode current I_a and I_C = collector current I_{C1}. Therefore, for Q_1

$I_{C1} = \alpha_1 I_a + I_{CBO1}$ ……..(4.3)

where α_1 = common-base current gain of Q_1

and I_{CBO1} = common-base leakage current of Q_1

Similarly, for transistor Q_2, the collector current I_{C2} is given by

$I_{C2} = \alpha_2 I_k + I_{CBO2}$ …(4.4)

where α_2 – common-base current gain of Q_2,I_{CBO2} =common-base leakage current of Q_2 and

I_k = emitter current of Q_2.

The sum of two collector currents given by Eqs. (4.3) and (4.4) is equal to the external circuit current I_α entering at anode terminal A.

There fore $I_a = I_{C1} + I_{C2}$

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \quad \ldots(4.5)$$

When gate current is applied, then $I_k = I_a + I_g$. Substituting this value of I_k in Eq. (4.5) gives

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

or

$$I_a = \alpha_2 I_g + I_{CBO1} + I_{CBO2} /[1-(\alpha_1 + \alpha_2)]$$

For a silicon transistor, current gain α is very low at low emitter current. With an increase in emitter current, a builds up rapidly as shown in Fig. 4.16. With gate current $I_g = 0$ and with thyristor forward biased,($\alpha_1 + \alpha_2$)is very low as per Eq (4.6) and forward leakage current somewhat more than $I_{CBO1} + I_{CBO2}$ flows. If, by some means, the emitter current of two component transistors can be increased so that $\alpha_1 + \alpha_2$ approaches unity, then as per Eq. (4.6) I_a would tend to become infinity thereby turning-on the device. Actually, external load limits the anode current to a safe value after the thyristor begins conduction. The methods of turning-on a thyristor, in fact, are the methods of making $\alpha_1 + \alpha_2$ to approach unity. These 0.25 various mechanisms for turning-on a thyristor are now discussed below :

(i) **GATE Triggering** : With anode positive with respect to cathode and with gate current $I_g = 0$, Eq. (4.6) shows that anode current, equal to the forward leakage current, is somewhat more than $I_{CBO1} + I_{CBO2}$,Under these conditions, the device is in the forward blocking state.

Now a sufficient gate-drive current between gate and cathode of the transistor is applied. This gate-drive current is equal to base current $I_{B2} = I_g$ and emitter current I_k of transistor Q_2. With the establishment of emitter current I_k of Q_2, current gain α_2 of Q_2 increases and base current I_{B2} causes the existence of collector current $I_{C2} = \beta_2 I_{B2} = \beta_2 I_g$. This amplified current I_{C2} serves as the base current I_{B1} of transistor Q_1 With the flow of I_{B1} collector current $I_{C1} = \beta_1 I_{B1} = \beta_1 \beta_2 I_g$ of Q_1comes into existence. Currents I_{B1} and I_{C1} lead to the establishment of emitter current I_a of Q_1 and this causes current gain α_1 to rise as desired. Now current $I_g + I_{CI} = (1 + \beta_1 \beta_2) I_g$ acts as the base current of Q_2 and therefore its emitter current $I_k = I_{CI} + I_g$ With the rise in emitter current I_k α_2 of Q_2 increases and this further causes $I_{C2} = P_2 (1 + \beta_1 \beta_2) I_g$ to rise. As amplified collector current I_{C2} is equal to the base current of Q_1 current gain α_1 eventually rises further. There is thus established a regenerative action internal to the device. This regenerative or positive feedback effect causes $\alpha_1 + \alpha_2$to grow towards unity. As a consequence, anode current begins to grow towards a larger value limited only by load impedance external to the device. When regeneration has grown sufficiently, gate current can be withdrawn. Even after $I_g$is removed, regeneration continues. This characteristic of the thyristor makes it suitable for pulse triggering. Note that thyristor is a latching device

After thyristor is turned on, all the four layers are filled with carriers and all junctions are forward biased. Under these conditions, thyristor has very low impedance and is in the forward on-state.

(ii) **Forward-voltage triggering** : If the forward anode to cathode voltage is increased, the collector to emitter voltages of both the transistors are also increased. As a result, the leakage current at the middle junction J_2 of thyristor increases, which is also the collector current of Q_2 as well as Q_1 With increase in collector currents I_{C1} and I_{C2} due to avalanche effect, the emitter currents of the two transistors also increase causing α_{1+} α_2 to approach unity. This leads to switching action of the device due to regenerative action. The forward-voltage triggering for turning-on a thyristor may be destructive and should therefore be avoided.

(iii) **dv/dt triggering** : The reversed biased junction J_2 behaves like a capacitor because of the space-charge present there. Let the capacitance of this junction be Cj. For any capacitor, i = C dv/dt.In case it is assumed that entire forward voltage v_a appears across reverse biased junction J_2 then charging current across the junction is given by

$i = Cj\ dv_a /dt$

This charging or displacement current across junction J_2 is collector currents of Q_2 and Q_1 Currents I_{C2}, I_{C1} will induce emitter current in Q_2, Q_1 In case rate of rise of anode voltage is large, the emitter currents will be large and as a result, α_{1+} α_2 will approach unity leading to eventual switching action of the thyristor.

(iid **Temperature triggering** : At high temperature, the forward leakage current across junction J_2 rises. This leakage current serves as the collector junction current of the component transistors Q_1 and Q_2. Therefore, an increase in leakage current I_{CI}, I_{C2} leads to an increase in the emitter currents of Q_l Q_2. As a result, (α_{1+} α_2) approaches unity. Consequently, switching action of thyristor takes place.

(v) **Light triggering** : When light is thrown on silicon, the electron-hole pairs increase. In the forward-biased thyristor, leakage current across J_2 increases which eventually increases α_{1+} α_2 to unity as explained before and switching action of thyristor occurs.

As stated before, gate-triggering is the most common method for turning-on a thyristor. Light-triggered thyristors are used in HVDC applications.

The operational differences between thyristor-family and transistor family of devices may now be summarised as under :

i) Once a thyristor is turned on by a gate signal, it remains latched in on-state due to internal regenerative action. However, a transistor must be given a continuous base signal to remain in on-state.

ii) In order to turn-off a thyristor, a reverse voltage must be applied across its anode-cathode terminals. However, a transistor turns off when its base signal is removed.

Different Firing Circuits of SCR:

One common application of the uni junction transistor is the triggering of the other devices such as the SCR, triac etc. The basic elements of such a triggering circuit are shown in figure. The resistor R_E is chosen so that the load line determined by R_E passes through the device characteristic in the negative resistance region, that is, to the right of the peak point but to the left of the valley point, as shown in figure. If the load line does not pass to the right of the peak point P, the device cannot turn on.

For ensuring turn-on of UJT

$R_E < V_{BB} - V_p / I_P$

This can be established as below

Consider the peak point at which $I_{RE} = I_p$ and $V_E = V_P$

(the equality $I_{RE} = I_P$ is valid because the charging current of capacitor, at this instant is zero, that is, the capacitor, at this particular instant, is changing from a charging state to a discharging state). Then $V_E = V_{BB} - I_{RE} R_E$

So, $R_{E(MAX)} = V_{BB} - V_E / I_{RE} = V_{BB} - V_p / I_P$ *at the peak point.*

At the valley point, V

$I_E = I_V$ and $V_E = V_V$ so that

$V_E = V_{BB} - I_{RE} R_E$

So $R_{E(MIN)} = V_{BB} - V_E / I_{RE} = V_{BB} - V_V / I_V$ or for ensuring turn-off.

$R_E > = V_{BB} - V_V / I_V$

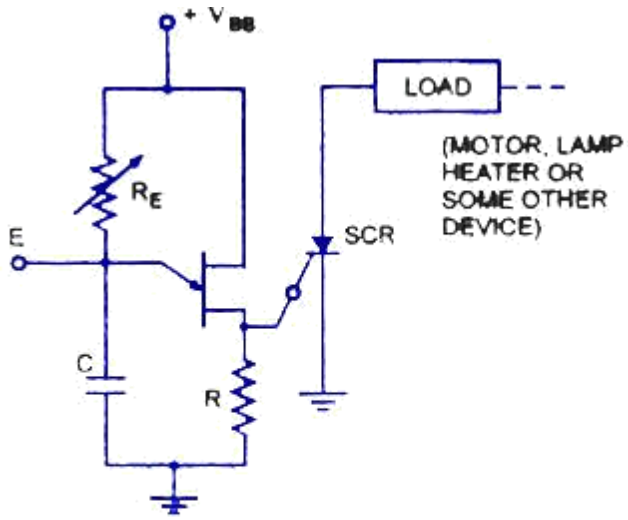
So, the range of resistor R_E is given as

$V_{BB} - V_P / I_P > R_E > V_{BB} - V_V / I_V$

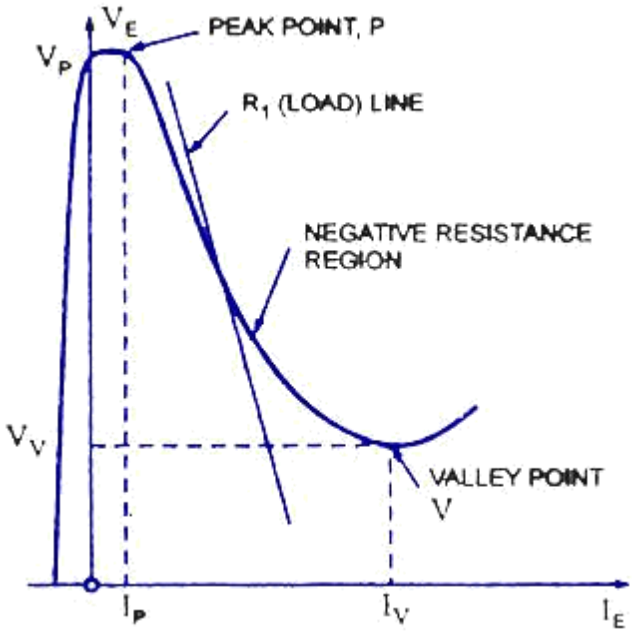
The resistor R is chosen small enough so as to ensure that SCR is not turned on by voltage V_R when emitter terminal E is open or $I_E = 0$

The voltage $V_R = RV_{BB}/R + R_{BB}$ for open-emitter terminal.

The capacitor C determines the time interval between triggering pulses and the time duration of each pulse. By varying R_E, we can change the time constant $R_E C$ and alter the point at which the UJT fires. This allows us to control the conduction angle of the SCR, which means the control of load current.



UJT Triggering of An SCR



Series and Parallel connections of SCRs

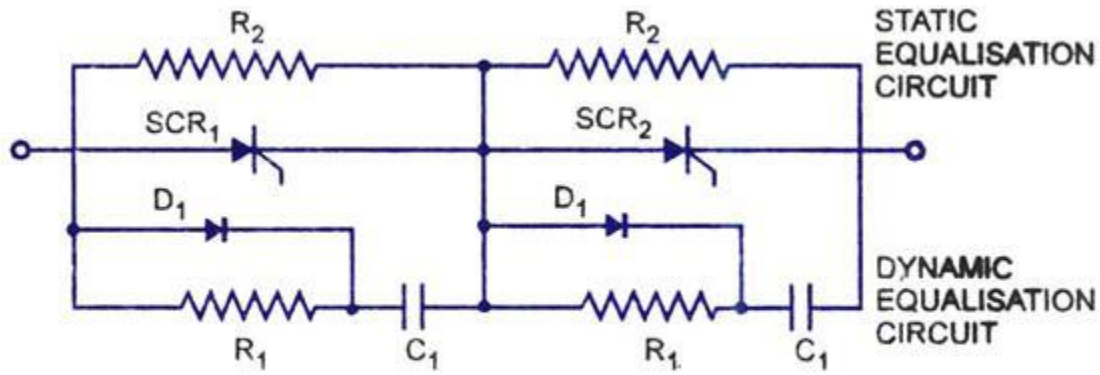
In many power control applications the required **voltage and current ratings** exceed the voltage and current that can be provided by a single SCR. Under such situations the SCRs are required to be connected in series or in parallel to meet the requirements. Sometimes even if the required rating is available, multiple connections are employed for reasons of economy and easy availability of SCRs of lower ratings.

Like any other electrical equipment, characteristics/properties of two SCRs of same make and ratings are never same and this leads to certain problems in the circuit. The mismatching of

SCRs is due to differences in

(i) turn-on time
(ii) turn-off time
(iii) leakage current in forward direction
(iv) leakage current in reverse direction and
(iii) recovery voltage.

Series Connection of an SCR



Equalisation For Series Connection

When the required voltage rating exceeds the SCR voltage rating, a number of SCRs are required to be connected in series to share the forward and reverse voltage. As it is not possible to have SCRs of completely identical characteristics, deviation in characteristics lead to the following two major problems during series connections of the SCRs:

***(i)* Unequal distribution of voltage across SCRs.**

***(ii)* Difference in recovery characteristics.**

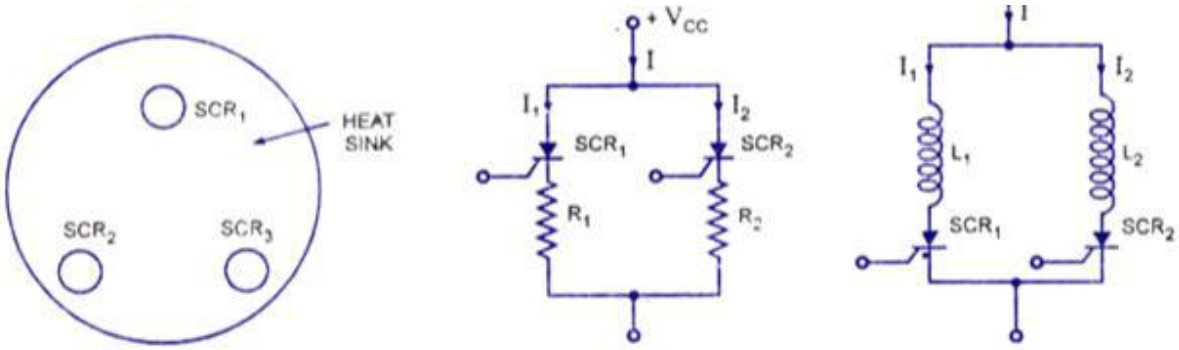
Care must be taken to share the voltage equally. For steady-state conditions, voltage sharing is achieved by using a resistance or a Zener diode in parallel with each SCR. For transient voltage sharing a low non-inductive resistor and capacitor in series are placed across each SCR, as shown in figure. Diodes D_1 connected in parallel with resistor R_l, helps in dynamic stabilisation. This circuit reduces differences between blocking voltages of the two devices within permissible limits. Additionally the R-C circuit can also serve the function of**'snubber circuit'**. Values of R_1 and C_1 can primarily be calculated for snubber circuit and a check can be made for equali-zation. If ΔQ is the difference in recovery charge of two devices arising out of different recovery current for different time and ΔV is the permissible difference in blocking voltage

then $C_1 = \Delta Q / \Delta V$.

The value of resistance R_X should be sufficient to over damp the circuit.

Since the capacitor C_1 can discharge through the SCR during turn-on, there can be excessive power dissipation, but the switching current from C_1 is limited by the resistor R_1 This resistance also serves the purpose of damping out 'ringing' which is oscillation of C_1 with the circuit inductance during commutation. All the SCRs connected in series should be turned-on at the same time when signals are applied to their gates simultaneously.

Parallel Connection of an SCR



When the load current exceeds the SCR current rating, SCRs are connected in parallel to share the load current. But when SCRs are operated in parallel, the current sharing between them may not be proper. The device having lower dynamic resistance will tend to share more current. This will raise the temperature of that particular device in comparison to other, thereby reducing further its dynamic resistance and increasing current through it. This process is cumulative and continues till the device gets punctured.

Some other factors which directly or indirectly add to this problem are difference in turn-on time, delay time, finger voltage* and loop inductance. Arrangement of SCRs in the cubicle also plays vital role. When the SCRs are connected in parallel, it must be ensured that the latching current level of the all the SCRs is such that when gate pulse is applied, all of them turn-on and remain on when the gate pulse is removed. Further the holding currents of the devices should not be so much different that at reduced load current one of the device gets turned-off because of fall of current through it blow its holding current value. This is particularly important because on increase in load current, the device which has stopped conducting cannot start in the absence of gate pulse.

Another point to be considered is the on-state voltage across the device. For equal sharing of currents by the devices voltage drop across the parallel paths must be equal. For operation of all the SCRs connected in parallel at the same temperature, it becomes necessary to use a common heat sink for their mounting, as illustrated in figure. Resistance compensation used for dc circuits is shown in figure. In this circuit the resistors R_X and R_2 are chosen so as to cause equal voltage drop in both arms. Inductive compensation used for ac circuits is shown in figure The difference in characteristics due to different turn-on time, delay time, finger voltage, latching current,

holding current can be minimized by using inductive compensation. Firing circuits giving high rate of rise can be used to reduce mismatch of gate characteristics and delay time.

Current sharing circuits must be designed so as to distribute current equally at maximum temperature and maximum anode current. This is done to ensure that the devices share current equally under worst operating conditions. Mechanical arrangement of SCRs also plays an important role in reducing mismatching. Cylindrical construction is perhaps the best from this point of view.

Derating. Even with all the measures taken, it is preferable to derate the device for series/parallel operation. Another reason for derating is poor cooling and heat dissipation as number of devices operate in the same branch of the circuit.

Normal derating factors are 10 to 15% for parallel connection of SCRs depending upon the number of devices connected in parallel. Higher voltage safety factor is taken when SCRs are connected in series.

Commutation circuits

- Requirements to be satisfied for the successful turn-off of a SCR
- The turn-off groups as per the General Electric classification
- The operation of the turn-off circuits
- Design of a SCR commutation circuit

A thyristor can be turned ON by applying a positive voltage of about a volt or a current of a few tens of milliamps at the gate-cathode terminals. However, the amplifying gain of this regenerative device being in the order of the 10^8, the SCR cannot be turned OFF via the gate terminal. It will turn-off only after the anode current is annulled either naturally or using forced commutation techniques. These methods of turn-off do not refer to those cases where the anode current is gradually reduced below Holding Current level manually or through a slow process. Once the SCR is turned ON, it remains ON even after removal of the gate signal, as long as a minimum current, the Holding Current, I_h, is maintained in the main or rectifier circuit.

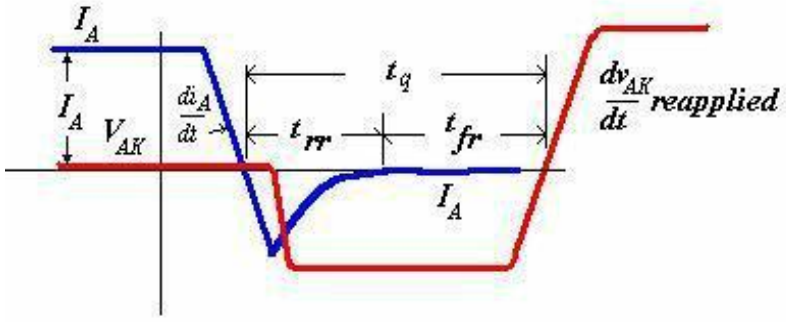


Fig. 3.1 Turn-off dynamics of the SCR

In all practical cases, a negative current flows through the device. This current returns to zero only after the reverse recovery time t_{rr}, when the SCR is said to have regained its reverse blocking capability. The device can block a forward voltage only after a further t_{fr}, the forward recovery time has elapsed. Consequently, the SCR must continue to be reverse-biased for a minimum of $t_{fr} + t_{rr} = t_q$, the rated turn- off time of the device. The external circuit must therefore

reverse bias the SCR for a time $t_{off} > t_q$. Subsequently, the reapplied forward biasing voltage must rise at a dv/dt < dv/dt (reapplied) rated. This dv/dt is less than the static counterpart. General Electric has suggested six classification methods for the turn-off techniques generally adopted for the SCR. Others have chosen different classification rules.

SCRs have turn-off times rated between 8 - 50 μsecs. The faster ones are popularly known as 'Inverter grade' and the slower ones as 'Converter grade' SCRs. The latter are available at higher current levels while the faster ones are expectedly costlier.

Classification of forced commutation methods

The six distinct classes by which the SCR can be turned off are:

Class A	Self commutated by a resonating load
Class B	Self commutated by an L-C circuit
Class C	C or L-C switched by another load carrying SCR
Class D	C or L-C switched by an auxiliary SCR

Class E An external pulse source for commutation Class
F AC line commutation

These examples show the classes as choppers. The commutation classes may be used in practice in configurations other than choppers.

Class A, Self commutated by resonating the load

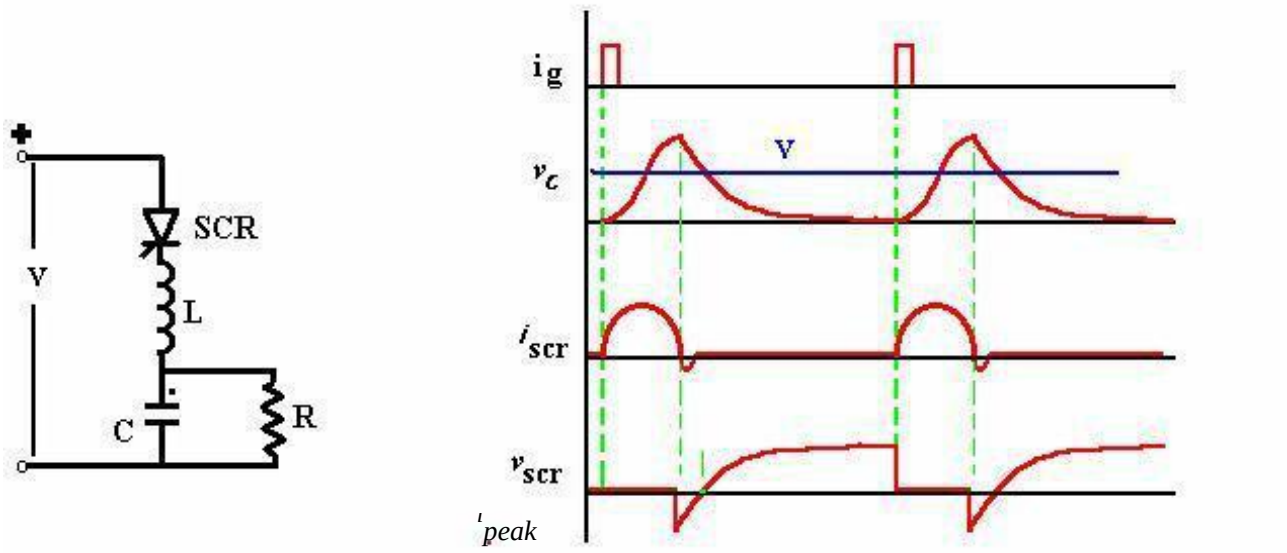


Fig. 3.2 A resonant load commutated SCR and the corresponding waveforms

When the SCR is triggered, anode current flows and charges up C with the dot as positive. The L-C-R form a second order under-damped circuit. The current through the SCR builds up and completes a half cycle. The inductor current will then attempt to flow through the SCR in the reverse direction and the SCR will be turned off.

The capacitor voltage is at its peak when the SCR turns off and the capacitor discharges into the resistance in an exponential manner. The SCR is reverse-biased till the capacitor voltages returns to the level of the supply voltage V.

Class B, Self commutated by an L-C circuit

The Capacitor C charges up in the dot as positive before a gate pulse is applied to the SCR. When SCR is triggered, the resulting current has two components.

The constant load current I_{load} flows through R - L load. This is ensured by the large reactance in series with the load and the freewheeling diode clamping it. A sinusoidal current flows through the resonant L- C circuit to charge-up C with the dot as negative at the end of the half cycle. This current will then reverse and flow through the SCR in opposition to the load current for a small fraction of the negative swing till the total current through the SCR becomes zero. The SCR will turn off when the resonant–circuit (reverse) current is just greater than the load current.

The SCR is turned off if the SCR remains reversed biased for $t_q > t_{off}$, and the rate of rise of the reapplied voltage < the rated value.

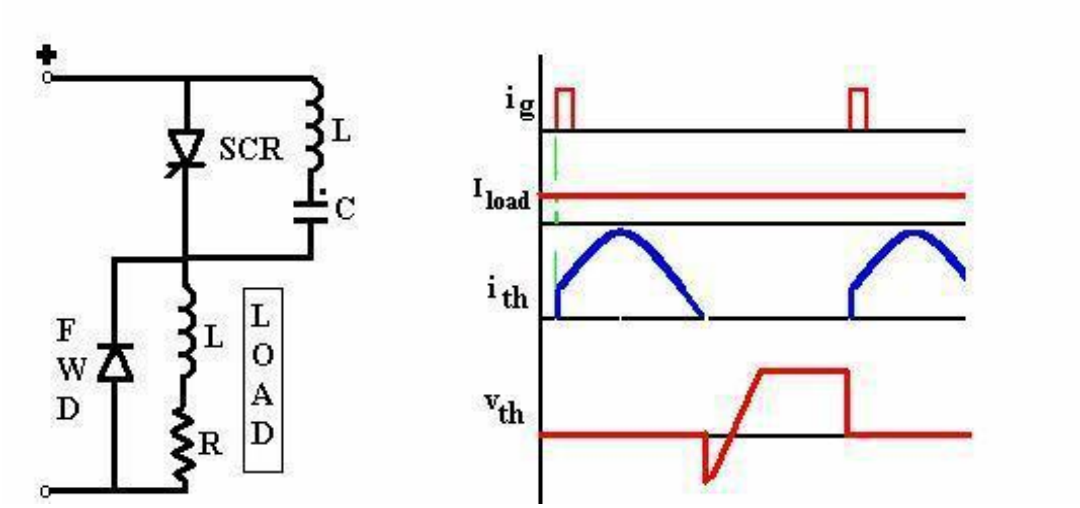


Fig. 3.3 Class B, L-C turn-off

Problem #1

A Class B turn-off circuit commutates an SCR. The load current is constant at 10 Amps. Dimension the commutating components L and C. The supply voltage is 100VDC.

Soln # 1

The commutating capacitor is charged to the supply voltage = 100 V

The peak resonant current is,

$$= V\sqrt{C/L}$$

Assuming, $i_{peak} \simeq 1.5.I_{load}$

$C/L = (15/100)^2 = 0.0225$

The SCR commutates when the total current through it reaches zero.This corresponds to 0.73 rads after the zero crossing of the resonant current. The capacitor voltage at that instant is 75 volts. After the SCR turns off, the capacitor is charged linearly by the load current.

If the SCR is to commutate at twice this load current, for a rated "Inverter grade' SCR turn-off time of 20 μsecs,

It can be observed that if the peak of the commutating current is just equal to the load current, the turn-off time would be zero as the capacitor would not be able to impress any negative voltage on the SCR.

Class C, C or L-C switched by another load–carrying SCR

This configuration has two SCRs. One of them may be the main SCR and the other auxiliary. Both may be load current carrying main SCRs. The configuration may have four SCRs with the load across the capacitor, with the integral converter supplied from a current source. Assume SCR_2 is conducting. C then charges up in the polarity shown. When SCR_1 is triggered, C is switched across SCR_2 via SCR_1 and the discharge current of C opposes the flow of load current in SCR_2.

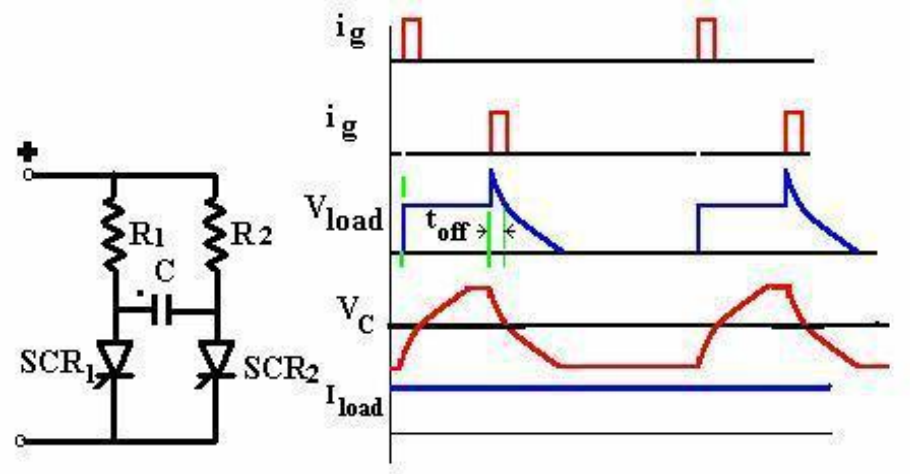


Fig. 3.4 Class C turn-off, SCR switched off by another load-carring SCR

Class D, L-C or C switched by an auxiliary SCR

Example 1

The circuit shown in Figure 3.3 (Class C) can be converted to Class D if the load current is carried by only one of the SCR's, the other acting as an auxiliary turn-off SCR. The auxiliary SCR would have a resistor in its anode lead of say ten times the load resistance.

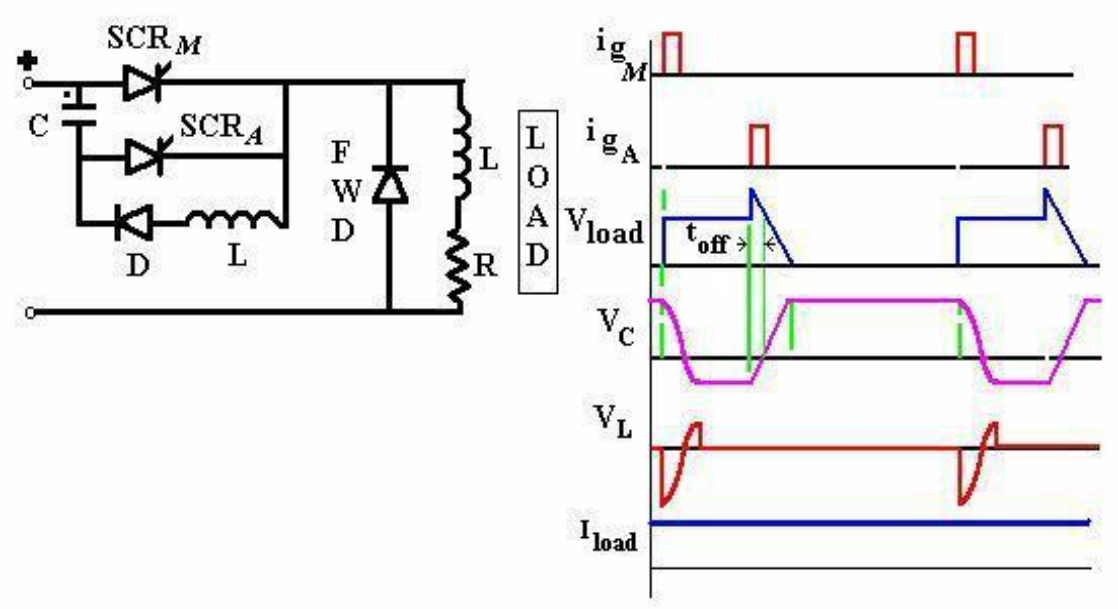


Fig. 3.5 Class D turn-off. Class D commutation by a C (or LC) switched by an Auxiliary SCR.

Example 2

SCR_A must be triggered first in order to charge the upper terminal of the capacitor as positive. As soon as C is charged to the supply voltage, SCR_A will turn off. If there is substantial inductance in the input lines, the capacitor may charge to voltages in excess of the supply voltage. This extra voltage would discharge through the diode-inductor-load circuit.

When SCR_M is triggered the current flows in two paths: Load current flows through the load and the commutating current flows through C- SCR_M -L-D network. The charge on C is reversed and held at that level by the diode D. When SCR_A is re-triggered, the voltage across C appears across SCR_M via SCR_A and SCR_M is turned off. If the load carries a constant current as in Fig. 3.4, the capacitor again charges linearly to the dot as positive.

Problem # 2

A Class D turn-off circuit has a commutating capacitor of 10 μF. The load consists of a clamped inductive load such that the load current is reasonably constant at 25 amperes. The 'Inverter grade' SCR has a turn-off time of 12 μsecs. Determine whether the SCR will be satisfactorily commutated. Also dimension the commutating inductor. The supply voltage is 220 VDC.

Soln # 2

The capacitor is initially charged to the supply voltage **220 V** at the end of the conduction period of SCR_A.

When SCR_M is triggered, the 25 Amps load current and the L-C ringing current flows through it. Peak current through SCR is

$$i_{peak} = 25 + 220\sqrt{C/L} \quad Amps$$

Selecting L such that $i_{peak} \sim 1.5$. load current,

$$\sqrt{C/L} = 25 = 0.0568\ L$$
$$2.220$$
$$L = 3.1 \quad mH$$

Assuming that the capacitor charges to 70% of its original charge because of losses in the C- SCR_M -L-D network, and it charges linearly when SCR_A is again triggered,

$$I_{load} .t_q = 10(0.7.220)10^{-6} = 1540.10^{-6}\ t$$
$$t_q = 1540 / 25 = 61.6\ \mu\text{sec}\ s$$

The SCR can therefore be successfully commutated.

The maximum current that can be commutated with the given Capacitor at the 220 V supply voltage is

$$I_{load} = 1540 / 12 = 128 \quad Amps$$

For the 25 Amps load current the capacitor just enough would have a rating of

$$C = I_{load} .t_q /(0.7.220) = (25.12) /154 = 1.95 \approx 2.0 \quad \mu F$$

If the supply voltage is reduced by a factor **K**, the required capacitor rating increases by the same factor **K** for the same load current**.**

Class E – External pulse source for commutation

The transformer is designed with sufficient iron and air gap so as not to saturate. It is capable of carrying the load current with a small voltage drop compared with the supply voltage.

When SCR1 is triggered, current flows through the load and pulse transformer. To turn SCR_1 off a positive pulse is applied to the cathode of the SCR from an external pulse generator via the pulse transformer. The capacitor C is only charged to about 1 volt and for the duration of the turn-off pulse it can be considered to have zero impedance. Thus the pulse from the transformer reverses the voltage across the SCR, and it supplies the reverse recovery current and holds the voltage negative for the required turn-off time.

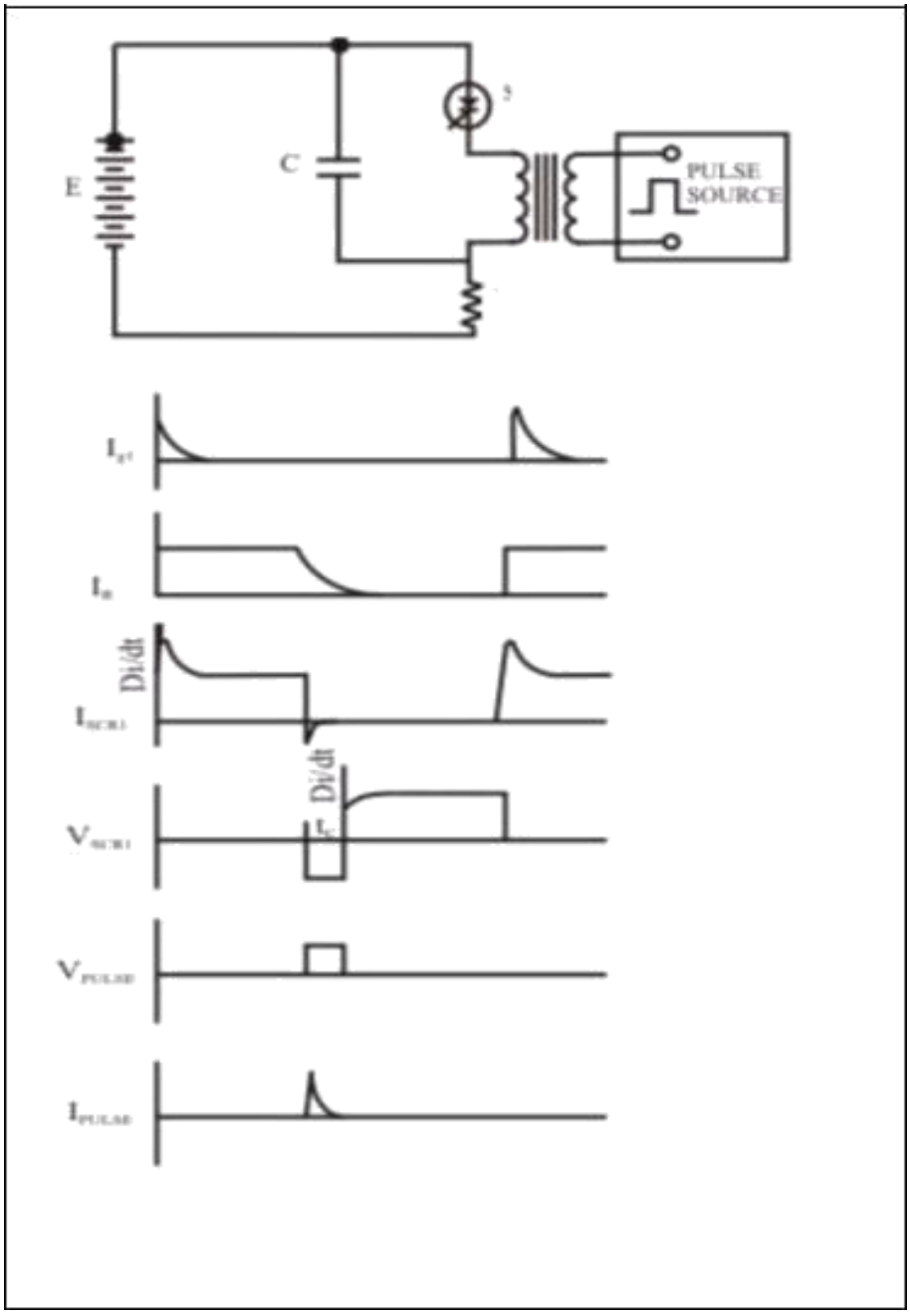


Fig. 3.6 Class E, External pulse commutation

Class F, AC line commutated

If the supply is an alternating voltage, load current will flow during the positive half cycle. With a highly inductive load, the current may remain continuous for some time till the

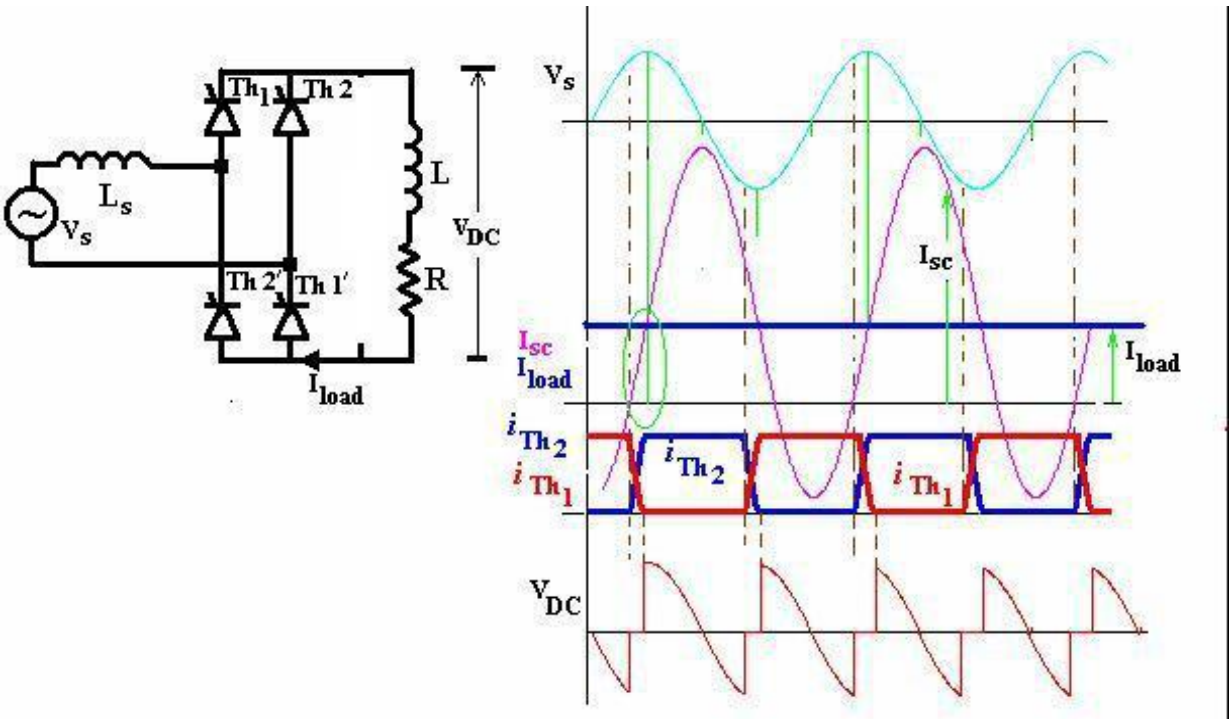


Fig. 3.7 Class F, natural commutation by supply voltage

energy trapped in the load inductance is dissipated. During the negative half cycle, therefore, the SCR will turn off when the load current becomes zero 'naturally'. The negative polarity of the voltage appearing across the outgoing SCR turns it off if the voltage persists for the rated turn-off period of the device. The duration of the half cycle must be definitely longer than the turn-off time of the SCR.

The rectifier in Fig.3.6 is supplied from an single phase AC supply. The commutation process involved here is representative of that in a three phase converter. The converter has an input inductance L_S arising manly out of the leakage reactance of the supply transformer. Initially, SCRs Th_1 and $Th_{1'}$ are considered to be conducting. The triggering angle for the converter is around 60^0. The converter is operating in the continuous conduction mode aided by the highly-inductive load.

When the incoming SCRs, Th_2 and $Th_{2'}$ are triggered, the current through the incoming devices cannot rise instantaneously to the load current level. A circulating current I_{sc} builds up in the short-circuited path including the supply voltage, V_s-L_s-$Th_{1'}$- Th_2 and V_s- L_s-$Th_{2'}$-Th_1 paths. This current can be described by:

$$I_{sc} = \frac{V_s \sin(\omega t - 90^0)}{\omega L_S} + \frac{V_s}{\omega L_S}\cos\alpha = \frac{V_s \cos(\omega t)}{\omega L_S} + \frac{V_s}{\omega L_S}\cos\alpha$$

where α the triggering angle and I_{sc} and V_s as shown in Fig. 3.6.

This expression is obtained with the simplifying assumption that the input inductance contains no resistances. When the current rises in the incoming SCRs, which in the outgoing

ones fall such that the total current remains constant at the load current level. When the current in the incoming ones reach load current level, the turn-off process of the outgoing ones is initiated. The reverse biasing voltage of these SCRs must continue till they reach their forward blocking state. As is evident from the above expression, the overlap period is a function of the triggering angle. It is lowest when $\alpha \sim 90^0$. These SCRs being 'Converter grade', they have a larger turn-off time requirement of about 30-50 μsecs.

The period when both the devices conduct is known as the 'overlap period'. Since all SCRs are in conduction, the output voltage for this period is zero. If the 'fully-controlled' converter in Fig. 3.7 is used as an inverter with triggering angles $> 90^0$, the converter triggering can be delayed till the 'margin angle' which includes the overlap angle and the turn-off time of the SCR - both dependent on the supply voltages.

Rate of rise of forward voltage, dv/dt

The junctions of any semiconductor exhibit some unavoidable capacitance. A changing voltage impressed on this junction capacitance results in a current, I = C dv/dt. If this current is sufficiently large a regenerative action may occur causing the SCR to switch to the on state. This regenerative action is similar to that which occurs when gate current is injected. The critical rate of rise of off-state voltage is defined as the maximum value of rate of rise of forward voltage which may cause switching from the off-state to the on-state.

Since dv/dt turn-on is non-destructive, this phenomenon creates no problem in applications in which occasional false turn -on does not result in a harmful affect at the load. Heater application is one such case. However, at large currents where dv/dt turn-on is accompanied by partial turn-on of the device area a high di/dt occurs which then may be destructive.

The majority of inverter applications, however, would result in circuit malfunction due to dv/dt turn-on. One solution to this problem is to reduce the dv/dt imposed by the circuit to a value less than the critical dv/dt of the SCR being used. This is accomplished by the use of a circuit similar to those in Figure 3.8 to suppress excessive rate of rise of anode voltage. Z represents load impedance and circuit impedance. Variations of the basic circuit is also shown where the section of the network shown replaces the SCR and the R-C basic snubber.

Since circuit impedances are not usually well defined for a particular application, the values of R and C are often determined by experimental optimization. A technique can be used to simplify snubber circuit design by the use of nomographs which enable the circuit designer to select an optimized R-C snubber for a particular set of circuit operating conditions.

Another solution to the dv/dt turn-on problem is to use an SCR with higher dv/dt turn-on problem is to use an SCR with higher dv/dt capability. This can be done by selecting an SCR designed specially for high dv/dt applications, as indicated by the specification sheet. Emitter shorting is a manufacturing technique used to accomplish high dv/dt capability.

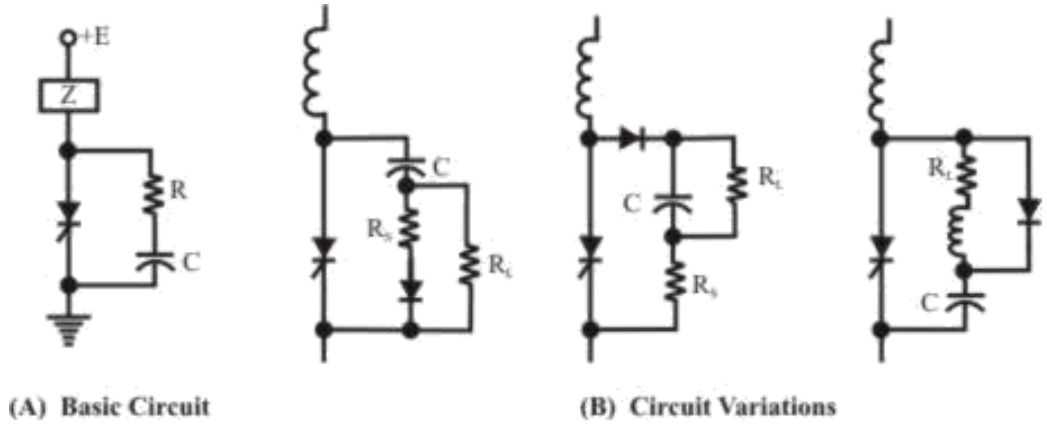


Fig. 3.8 dv/dt supression circuits

Questions

#1 For a Class D turn-off SCR, the load consists of a resistance only. If the supply voltage and SCR turn-off ratings are as in Problem # 1 calculate the required value of the commutating capacitor.

Ans: (Hints): The capacitor would now charge in an exponential manner. The time it takes to discharge from its reverse charged state once SCR_A is triggered is the circuit turn-off time which must be in excess of the rated 12 μsecs.

#2 For a Class F converter, will the overlap period rise with the leakage inductance of the converter? What happens to the output voltage?

Ans: Yes. The overlap time is directly related to the commutating inductance. The output voltage decreases. In fact, this inductor limits the maximum output current of the converter. The input current maximum would be as for a shorted network with the leakage inductance only present.

#3 Can the output DC voltage be controlled in the above circuits?

Ans: Yes. Most of the above circuits are also called 'forced commutated' DC-DC chopper circuits.

MODULE 4

Operation and analysis of single phase half controlled converters

Instructional Objectives

On completion the student will be able to

- Draw different topologies of single phase half controlled converter.
- Identify the design implications of each topology.
- Construct the conduction table and thereby draw the waveforms of different system variables in the continuous conduction mode of operation of the converter.
- Analyze the operation of the converter in the continuous conduction mode to find out the average and RMS values of different system variables.
- Find out an analytical condition for continuous conduction relating the load parameters with the firing angle.
- Analyze the operation of the converter in the discontinuous conduction mode of operation.

Introduction

Single phase fully controlled bridge converters are widely used in many industrial applications. They can supply unidirectional current with both positive and negative voltage polarity. Thus they can operate either as a controlled rectifier or an inverter. However, many of the industrial application do not utilize the inverter mode operation capability of the fully controlled converter. In such situations a fully controlled converter with four thyristors and their associated control and gate drive circuit is definitely a more complex and expensive proposition. Single phase fully

controlled converters have other disadvantages as well such as relatively poor output voltage (and current for lightly inductive load) form factor and input power factor.

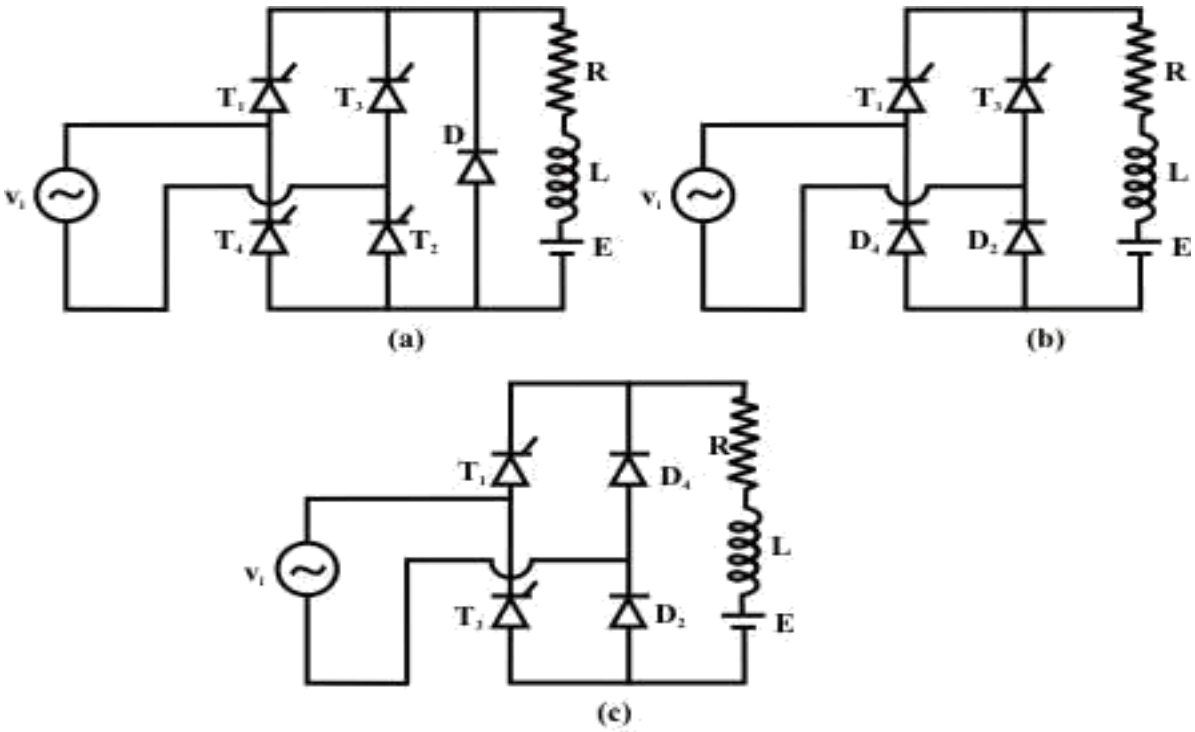


Fig. 11.1: Alternative circuits of single phase half controlled converter.
(a) fully controlled converter with load side free wheeling diode
(b) half controlled converter - alternative -1
(c) half controlled converter - alternative -2.

The inverter mode of operation of a single phase fully controlled converter is made possible by the forward voltage blocking capability of the thyristors which allows the output voltage to go negative. The disadvantages of the single phase fully controlled converter are also related to the same capability. In order to improve the output voltage and current form factor the negative excursion of the output voltage may be prevented by connecting a diode across the output as shown in Fig 11.1(a). Here as the output voltage tries to go negative the diode across the load becomes forward bias and clamp the load voltage to zero. Of course this circuit will not be able to operate in the inverter mode. The complexity of the circuit is not reduced, however. For that, two of the thyristors of a single phase fully controlled converter has to be replaced by two diodes as shown in Fig 11.1 (b) and (c) . The resulting converters are called single phase half controlled converters. As in the case of fully controlled converters, the devices T_1 and D_2 conducts in the positive input voltage half cycle after T_1 is turned on. As the input voltage passes through negative going zero crossing D_4 comes into conduction commutating D_2 in Fig 11.1 (b) or T_1 in Fig 11.1 (c). The load voltage is thus clamped to zero until T_3 is fired in the negative half cycle. As far as the input and output behavior of the circuit is concerned the circuits in Fig 11.1
(b) and (c) are identical although the device designs differs. In Fig 11.1 (c) the diodes carry current for a considerably longer duration than the thyristors. However, in Fig 11.1 (b) both the thyristors and the diodes carry current for half the input cycle. In this lesson the operating principle and characteristics of a single phase half controlled converter will be presented with reference to the circuit in Fig 11.1 (b).

DEVICE / Mode	V_{T_1}	V_{T_3}	V_{D_2}	V_{D_4}	V_o
T_1D_2	0	$-V_i$	0	$-V_i$	V_i
T_1D_4	0	$-V_i$	V_i	0	0
T_3D_4	V_i	0	V_i	0	$-V_i$
T_3D_2	V_i	0	0	$-V_i$	0
NONE	$\frac{V_i - E}{2}$	$-\frac{V_i + E}{2}$	$\frac{V_i - E}{2}$	$-\frac{V_i + E}{2}$	E

Fig. 11.2: Conduction Table of single phase half controlled converter

Operating principle of a single phase half controlled bridge converter

With reference of Fig 11.1 (b), it can be stated that for any load current to flow one device from the top group (T_1 or T_3) and one device from the bottom group must conduct. However, T_1 T_3 or D_2 D_4 cannot conduct simultaneously. On the other hand T_1 D_4 and T_3 D_2 conducts simultaneously whenever T_1 or T_3 are on and the output voltage tends to go negative. Therefore, there are four operating modes of this converter when current flows through the load. Of course it is always possible that none of the four devices conduct. The load current during such periods will be zero. The operating modes of this converter and the voltage across different devices during these operating modes are shown in the conduction table of Fig 11.2. This table has been prepared with reference to Fig 11.1 (b).

It is observed that whenever D_2 conducts the voltage across D_4 is $-v_i$ and whenever D_4 conducts the voltage across D_2 is v_i. Since diodes can block only negative voltage it can be concluded that D_2 and D_4 conducts in the positive and the negative half cycle of the input supply respectively. Similar conclusions can be drawn regarding the conduction of T_1 and T_3. The operation of the converter can be explained as follows when T_1 is fired in the positive half cycle of the input voltage. Load current flows through T_1 and D_2. If at the negative going zero crossing of the input voltage load current is still positive it commutates from D_2 to D_4 and the load voltage becomes zero. If the load current further continuous till T_3 is fired current commutates from T_1 to T_3. This mode of conduction when the load current always remains above zero is called the continuous conduction mode. Otherwise the mode of conduction becomes discontinuous.

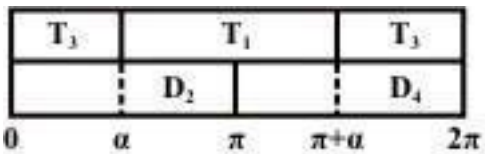
Fill in the blanks(s) with the appropriate word(s)

- In a half controlled converter two _____ of a fully controlled converter are replaced by two _____.
- Depending on the positions of the _____ the half controlled converter can have _____ different circuit topologies.
- The input/output waveforms of the two different circuit topologies of a half controlled converter are _____ while the device ratings are
  - _____.
- A half controlled converter has better output voltage _____ compared to a fully controlled converter.
- A half controlled converter has improved input _____ compared to a fully controlled converter.

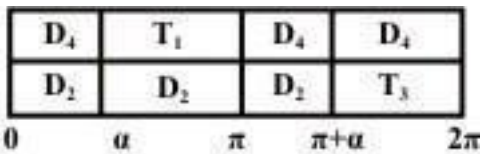
Answer: (i) thyristors, diodes; (ii) diodes, two; (iii) same, different; (iv) form factor; (v) power factor.

Find out an expression of the ration of the thyristor to diode RMS current ratings in the single phase half controlled converter topologies of Fig. 11.1(b) & (c). Assume ripple free continuous output current.

Answer



Conduction diagram of the circuit in Fig. 11.1(b).



Conduction diagram of the circuit in Fig. 11.1(c).

In the first conduction diagram the diodes and the thyristors conduct for equal periods, since the load current is constant. The ration of the thyristors to the diode RMS current ratings will be unity for the circuit of Fig 11.1 (b).

From the second conduction diagram the thyristors conduct for π - α radians while the diodes conduct for $\pi + \alpha$ radians. Since the load current is constant.

$$\frac{\text{Thyristor RMS current rating}}{\text{Diode RMS current rating}} = \sqrt{\frac{1-\alpha/\pi}{1+\alpha/\pi}}$$

in this case

Single phase half controlled converter in the continuous conduction mode

From the conduction table and the discussion in the previous section it can be concluded that the diode D_2 and D_4 conducts for the positive and negative half cycle of the input voltage waveform respectively. On the other hand T_1 starts conduction when it is fired in the positive half cycle of the input voltage waveform and continuous conduction till T_3 is fired in the negative half cycle.

Fig. 11.3 shows the circuit diagram and the waveforms of a single phase half controlled converter supplying an R – L – E load.

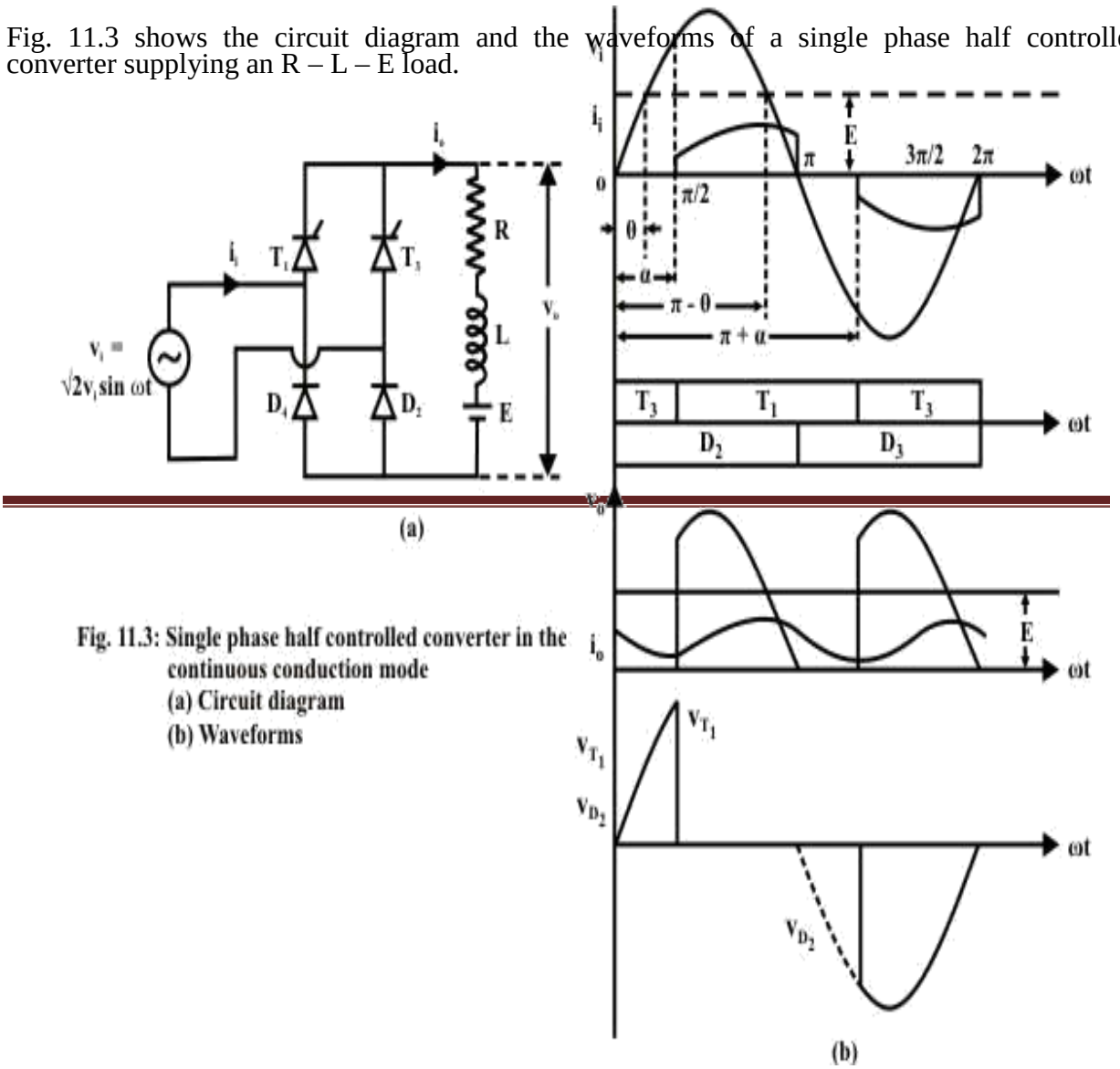
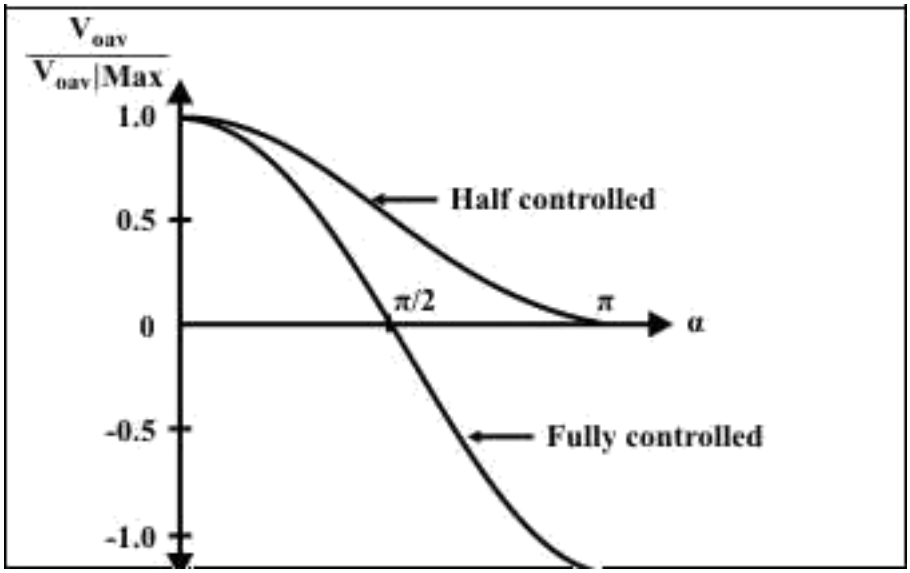


Fig. 11.3: Single phase half controlled converter in the continuous conduction mode
(a) Circuit diagram
(b) Waveforms

Referring to Fig 11.3 (b) T_1 D_2 starts conduction at $\omega t = \alpha$. Output voltage during this period becomes equal to v_i . At $\omega t = \pi$ as v_i tends to go negative D $_4$ is forward biased and the load current commutates from D_2 to D_4 and freewheels through D_4 and T_1. The output voltage remains clamped to zero till T_3 is fired at $\omega t = \pi + \alpha$. The T_3 D_4 conduction mode continues upto $\omega t = 2\pi$. Where upon load current again free wheels through T_3 and D_2 while the load voltage is clamped to zero.

From the discussion in the previous paragraph it can be concluded that the output voltage (hence the output current) is periodic over half the input cycle. Hence



Clearly in addition to the average component, the output voltage (and current) contains a large number of harmonic components. The minimum harmonic voltage frequency is twice the input supply frequency. Magnitude of the harmonic voltages can be found by Fourier series analysis of the load voltage and is left as an exercise.

The Fourier series representation of the load current can be obtained from the load voltage by applying superposition principle in the same way as in the case of a fully controlled converter.

However, the closed form expression of i_o can be found as explained next.

In the period $\alpha \leq \omega t \leq \pi$

The input current i_i is given by

$$\begin{aligned} ii &= i0 && \text{for } \alpha \leq \omega t \leq \pi \\ ii &= -i0 && \text{for } \pi + \alpha \leq \omega t \leq 2\pi \\ i_i &= 0 && \text{otherwise} \end{aligned} \qquad (11.14)$$

However, it will be very difficult to find out the characteristic parameters of i_i using equation 11.14 since the expression of i_0 is considerably complex. Considerable simplification can however be obtained if the actual i_i waveform is replaced by a quasisquare wave current waveform with an amplitude of I_{oav} as shown in Fig 11.5.

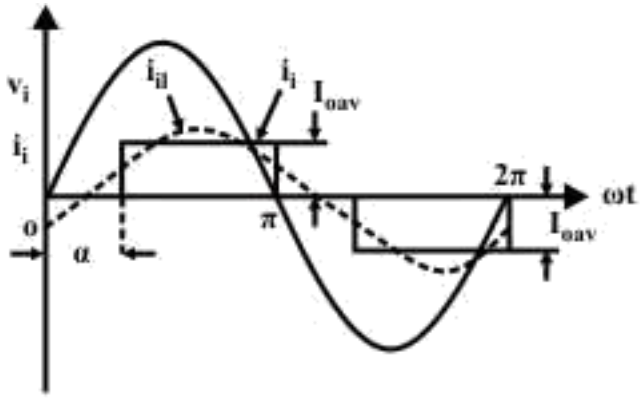


Fig. 11.5: Input current waveform of half controlled converters

Single phase half controlled converter in the discontinuous conduction mode.

So far we have discussed the operating characteristics of a single phase half controlled converter in the continuous conduction mode without identifying the condition required to achieve it. Such a condition exists however and can be found by carefully examining the way this converter works.

Referring to Fig 11.3 (b), when T_1 is fired at $\omega t = \alpha$ the output voltage (instantaneous value) is larger than the back emf. Therefore, the load current increases till v_o becomes equal to E again at $\omega t = \pi - \theta$. There, onwards the load current starts decreasing. Now if i_o becomes zero before T_3 is fired at $\omega t = \pi + \alpha$ the conduction becomes discontinuous. So clearly the condition for continuous conduction will be

If the condition in Eq. 11.22 is violated the conduction will become discontinuous. Clearly, two possibilities exist. In the first case the load current becomes zero before $\omega t = \pi$. In the second case i_o continuous beyond $\omega t = \pi$ but becomes zero before $\omega t = \pi + \alpha$. In both cases however, i_o starts from zero at $\omega t = \alpha$.

Fig. 11.6 shows the wave forms in these two cases.

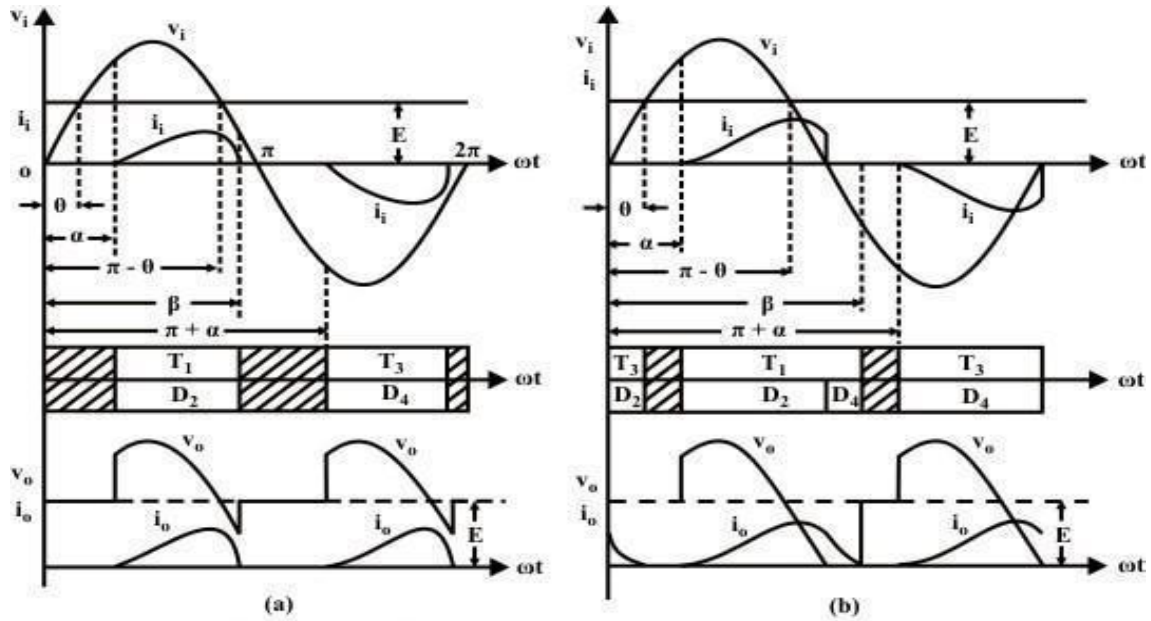


Fig. 11.6: Single phase half controlled converter in discontinuous conduction mode.
(a) $\pi - \theta \leq \beta \leq \pi$;
(b) $\pi \leq \beta \leq \pi + \alpha$

Of these two cases the second one will be analyzed in detail here. The analysis of the first case is left as an exercise.

For this case

$$\begin{aligned} v_o &= v_i && \text{for } \alpha \le \omega t \le \pi \\ v_o &= 0 && \text{for } \pi \le \omega t \le \beta \\ v_o &= E && \text{for } \beta \le \omega t \le \pi + \alpha \end{aligned} \qquad (11.23)$$

However I_{ORMS} cannot be computed directly from V_{ORMS}. For this the closed form expression for i_o has to be obtained. This will also help to find out an expression for the conduction angle β.

Fill in the blank(s) with the appropriate word(s).

(iv) At the boundary between continuous and discontinuous conduction the value of the output current at $\omega t = \alpha$ is _____.

(v) The output voltage and current waveform of a single phase fully controlled and half controlled converter will be same provided the extinction angle β is less than _____.

(vi) For the same value of the firing angle the average output voltage of a single phase half controlled converter is _____ in the discontinuous conduction mode compared to the continuous conduction mode.

(vii) Single phase half controlled converters are most suitable for loads requiring _____ voltage and current.

Answer: (i) zero; (ii) π; (iii) higher; (iv) unidirectional.

2. A single phase half controlled converter charges a 48v 50Ah battery from a 50v, 50Hz single phase supply through a 50mH line inductor. The battery has on interval resistance of 0.1Ω. The firing angle of the converter is adjusted such that the battery is charged at C/5 rate when it is fully discharged at 42 volts. Find out whether the conduction will be continuous or discontinuous at this condition. Up to what battery voltage will the conduction remain continuous? If the charging current of the battery is to become zero when it is fully charged at 52 volts what should be the value of the firing angle.

Lesson Summary

- Single phase half controlled converters are obtained from fully controlled converters by replacing two thyristors by two diodes.
- Two thyristors of one phase leg or one group (top or bottom) can be replaced resulting in two different topologies of the half controlled converter. From the operational point of view these two topologies are identical.
- In a half controlled converter the output voltage does not become negative and hence the converter cannot operate in the inverter mode.

- For the same firing angle and input voltage the half controlled converter in the continuous conduction mode gives higher output voltage compared to a fully controlled converter.
- For the same input voltage, firing angle and load parameters the half controlled converter has better output voltage and current form factor compared to a fully controlled converter.
- For the same firing angle and load current the half controlled converter in the continuous conduction mode has better input power factor compared to a fully controlled converter.
- Half controlled converters are most favored in applications requiring unidirectional output voltage and current.

Practice Problems and Answers

Q1. The thyristor T_3 of Fig 1.1(b) fails to turn on at the desired instant. Describe how this circuit will work in the presence of the fault.

Q2. A single phase half controlled converter is used to boost the no load speed of a separately excited dc machine by weakening its field supply. At $\alpha = 0°$ the half controlled converter produces the rated field voltage. If the field inductance is large enough to make the field current almost ripple face what will be the input power factor when the dc motor no load speed is bossed to 150%?

Q3. A single phase half controlled converter supplies a 220V, 1500rpm, 20A dc motor from a 230V 50HZ single phase supply. The motor has a armature resistance of 1.0Ω and inductance of 50mH. What will be the operating modes and torques for $\alpha = 30°$; and speed of 1400 RPM.

Operation and Analysis of single phase fully controlled converter.

Instructional Objectives

On completion the student will be able to

- Differentiate between the constructional and operation features of uncontrolled and controlled converters
- Draw the waveforms and calculate their average and RMS values of different variables associated with a single phase fully controlled half wave converter.
- Explain the operating principle of a single phase fully controlled bridge converter.
- Identify the mode of operation of the converter (continuous or discontinuous) for a given load parameters and firing angle.
- Analyze the converter operation in both continuous and discontinuous conduction mode and there by find out the average and RMS values of input/output, voltage/currents.
- Explain the operation of the converter in the inverter mode.

Introduction

Single phase uncontrolled rectifiers are extensively used in a number of power electronic based converters. In most cases they are used to provide an intermediate unregulated dc voltage source which is further processed to obtain a regulated dc or ac output. They have, in general, been proved to be efficient and robust power stages. However, they suffer from a few disadvantages. The main among them is their inability to control the output dc voltage / current magnitude when the input ac voltage and load parameters remain fixed. They are also unidirectional in the sense that they allow electrical power to flow from the ac side to the dc side only. These two disadvantages are the direct consequences of using power diodes in these converters which can block voltage only in one direction. As will be shown in this module, these two disadvantages are overcome if the diodes are replaced by thyristors, the resulting converters are called fully controlled converters.

Thyristors are semicontrolled devices which can be turned ON by applying a current pulse at its gate terminal at a desired instance. However, they cannot be turned off from the gate terminals. Therefore, the fully controlled converter continues to exhibit load dependent output voltage / current waveforms as in the case of their uncontrolled counterpart. However, since the thyristor can block forward voltage, the output voltage / current magnitude can be controlled by controlling the turn on instants of the thyristors. Working principle of thyristors based single phase fully controlled converters will be explained first in the case of a single thyristor halfwave rectifier circuit supplying an R or R-L load. However, such converters are rarely used in practice.

Full bridge is the most popular configuration used with single phase fully controlled rectifiers. Analysis and performance of this rectifier supplying an R-L-E load (which may represent a dc motor) will be studied in detail in this lesson.

Single phase fully controlled halfwave rectifier

4.3.1 Resistive load

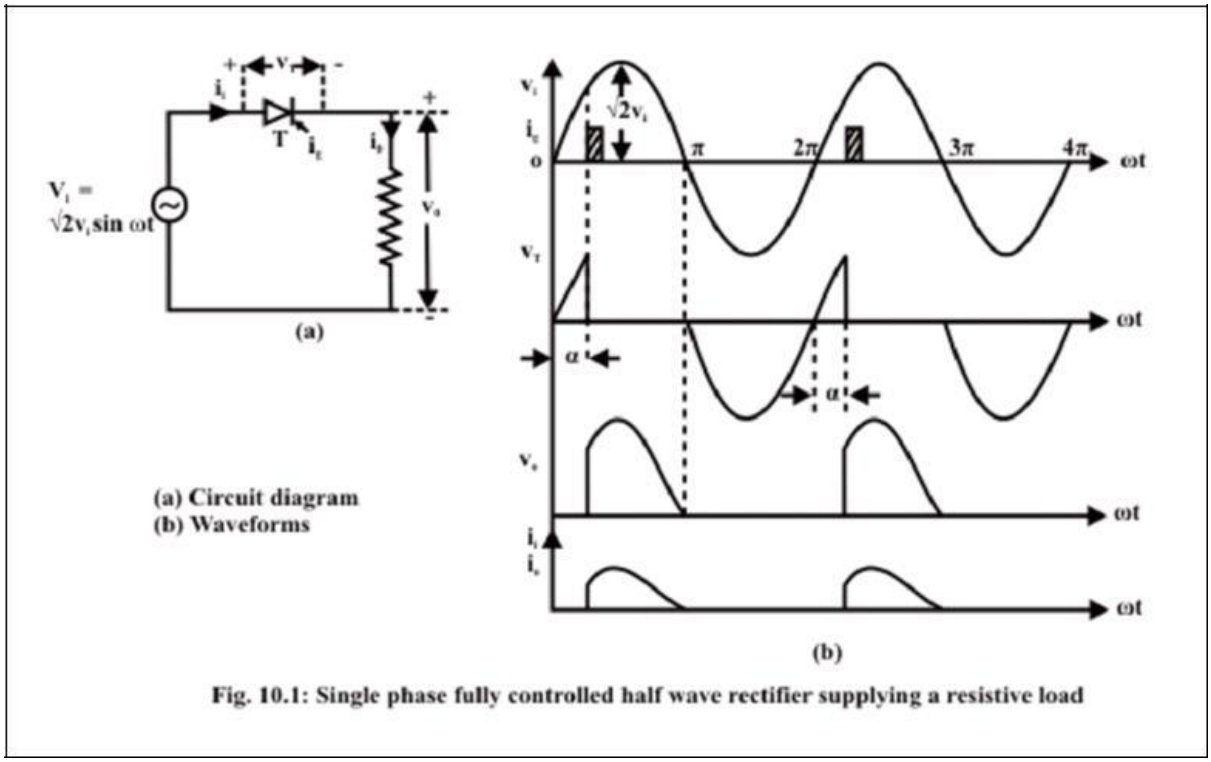
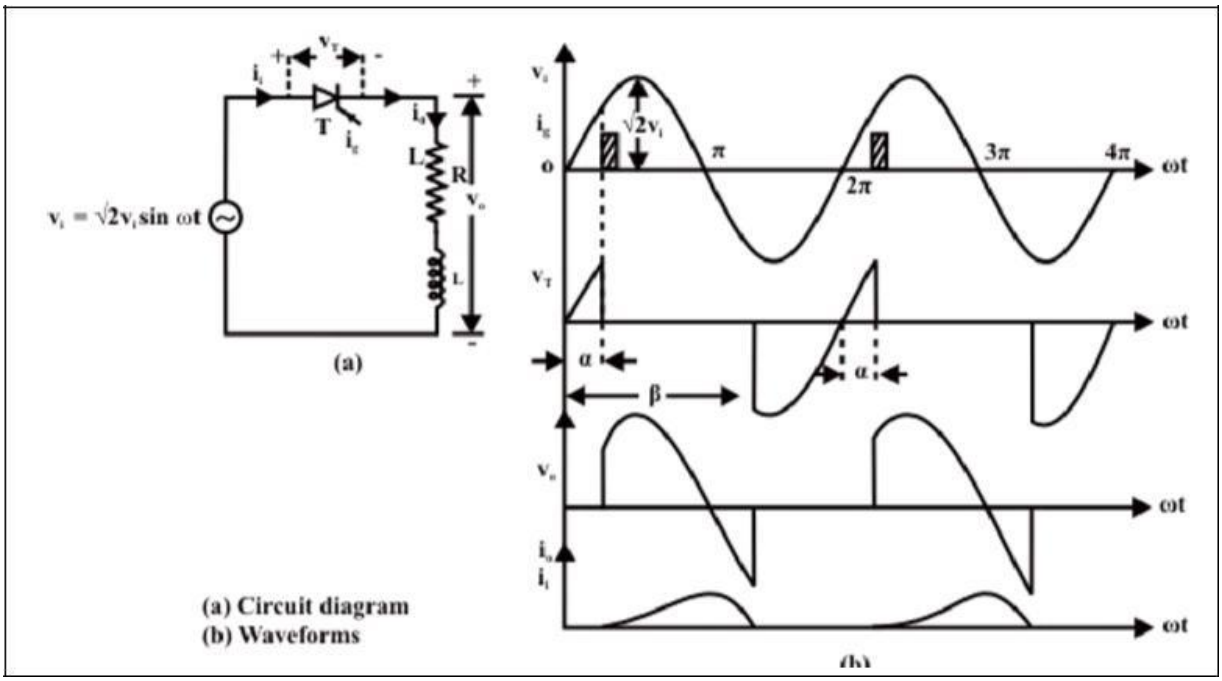


Fig. 10.1: Single phase fully controlled half wave rectifier supplying a resistive load

Fig.10. 1(a) shows the circuit diagram of a single phase fully controlled halfwave rectifier supplying a purely resistive load. At $t = 0$ when the input supply voltage becomes positive the thyristor T becomes forward biased. However, unlike a diode, it does not turn ON till a gate pulse is applied at $t = \alpha$. During the period $0 < t < \alpha$, the thyristor blocks the supply voltage and the load voltage remains zero as shown in fig 10.1(b). Consequently, no load current flows during this interval. As soon as a gate pulse is applied to the thyristor at $t = \alpha$ it turns ON. The voltage across the thyristor collapses to almost zero and the full supply voltage appears across the load. From this point onwards the load voltage follows the supply voltage. The load being purely resistive the load current i_O is proportional to the load voltage. At $t = \pi$ the supply voltage passes through the negative going zero crossing the load voltage and hence the load current becomes zero and tries to reverse direction. In the process the thyristor undergoes reverse recovery and starts blocking the negative supply voltage. Therefore, the load voltage and the load current remains clamped at zero till the thyristor is fired again at $t = 2\pi + \alpha$. The same process repeats there after.

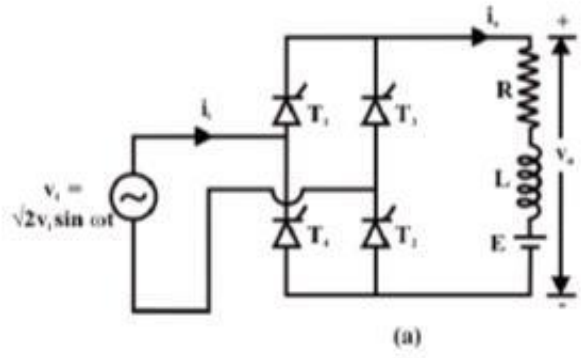
Resistive-Inductive load

Fig 10.2 (a) and (b) shows the circuit diagram and the waveforms of a single phase fully controlled halfwave rectifier supplying a resistive inductive load. Although this circuit is hardly used in practice its analysis does provide useful insight into the operation of fully controlled rectifiers which will help to appreciate the operation of single phase bridge converters to be discussed later.



As in the case of a resistive load, the thyristor T becomes forward biased when the supply voltage becomes positive at $\omega t = 0$. However, it does not start conduction until a gate pulse is applied at $\omega t = \alpha$ As the thyristor turns ON at $\omega t = \alpha$ the input voltage appears across the load and the load current starts building up. However, unlike a resistive load, the load current does not become zero at $t = \pi$, instead it continues to flow through the thyristor and the negative supply voltage appears across the load forcing the load current to decrease. Finally, at β ($\beta > \pi$) the load current becomes zero and the thyristor undergoes reverse recovery. From this point onwards the thyristor starts blocking the supply voltage and the load voltage remains zero until the thyristor is turned ON again in the next cycle. It is to be noted that the value of β depends on the load parameters. Therefore, unlike the resistive load the average and RMS output voltage depends on the load parameters. Since the thyristors does not conduct over the entire input supply cycle this mode of operation is called the "discontinuous conduction mode".

Single phase fully controlled bridge converter



MODE / DEVICE	T_1	T_2	T_3	T_4	v_o
T_1T_2	0	0	$-v_i$	$-v_i$	v_i
T_3T_4	v_i	v_i	0	0	$-v_i$
NONE	$\frac{v_i - E}{2}$	$\frac{v_i + E}{2}$	$-\frac{v_i + E}{2}$	$-\frac{v_i + E}{2}$	E

Fig 10.3: Single phase fully controlled bridge converter supplying an R - L - E load. (a) Circuit diagram, (b) Conduction table

Fig 10.3 (a) shows the circuit diagram of a single phase fully controlled bridge converter. It is one of the most popular converter circuits and is widely used in the speed control of separately excited dc machines. Indeed, the R-L-E load shown in this figure may represent the electrical equivalent circuit of a separately excited dc motor.

The single phase fully controlled bridge converter is obtained by replacing all the diode

of the corresponding uncontrolled converter by thyristors. Thyristors T_1 and T_2 are fired together while T_3 and T_4 are fired 180° after T_1 and T_2. From the circuit diagram of Fig 10.3(a) it is clear that for any load current to flow at least one thyristor from the top group (T_1, T_3) and one thyristor from the bottom group (T_2, T_4) must conduct. It can also be argued that neither T_1T_3 nor T_2T_4 can conduct simultaneously. For example whenever T_3 and T_4 are in the forward blocking state and a gate pulse is applied to them, they turn ON and at the same time a negative voltage is applied across T_1 and T_2 commutating them immediately. Similar argument holds for T_1 and T_2.

For the same reason T_1T_4 or T_2T_3 can not conduct simultaneously. Therefore, the only possible conduction modes when the current i_0 can flow are T_1T_2 and T_3T_4. Of coarse it is possible that at a given moment none of the thyristors conduct. This situation will typically occur when the load current becomes zero in between the firings of T_1T_2 and T_3T_4. Once the load current becomes zero all thyristors remain off. In this mode the load current remains zero. Consequently the converter is said to be operating in the discontinuous conduction mode.

Fig 10.3(b) shows the voltage across different devices and the dc output voltage during

each of these conduction modes. It is to be noted that whenever T_1 and T_2 conducts, the voltage across T_3 and T_4 becomes $-v_i$. Therefore T_3 and T_4 can be fired only when v_i is negative i.e, over the negative half cycle of the input supply voltage. Similarly T_1 and T_2 can be fired only over the positive half cycle of the input supply. The voltage across the devices when none of the thyristors conduct depends on the off state impedance of each device. The values listed in Fig 10.3 (b) assume identical devices.

Under normal operating condition of the converter the load current may or may not remain zero over some interval of the input voltage cycle. If i_0 is always greater than zero then the converter is said to be operating in the continuous conduction mode. In this mode of operation of the converter T_1T_2 and T_3T_4 conducts for alternate half cycle of the input supply. However, in the discontinuous conduction mode none of the thyristors conduct over some portion of the input cycle. The load current remains zero during that period.

Operation in the continuous conduction mode

As has been explained earlier in the continuous conduction mode of operation i_0 never becomes zero, therefore, either T_1T_2 or T_3T_4 conducts. Fig 10.4 shows the waveforms of different variables in the steady state. The firing angle of the converter is α. The angle θ is given by

It is assumed that at $t = 0^-$ T_3T_4 was conducting. As T_1T_2 are fired at $\omega t = \alpha$ they turn on commutating T_3T_4 immediately. T_3T_4 are again fired at $\omega t = \pi + \alpha$ Till this point T_1T_2 conducts. The period of conduction of different thyristors are pictorially depicted in the second waveform (also called the conduction diagram) of Fig 10.4.

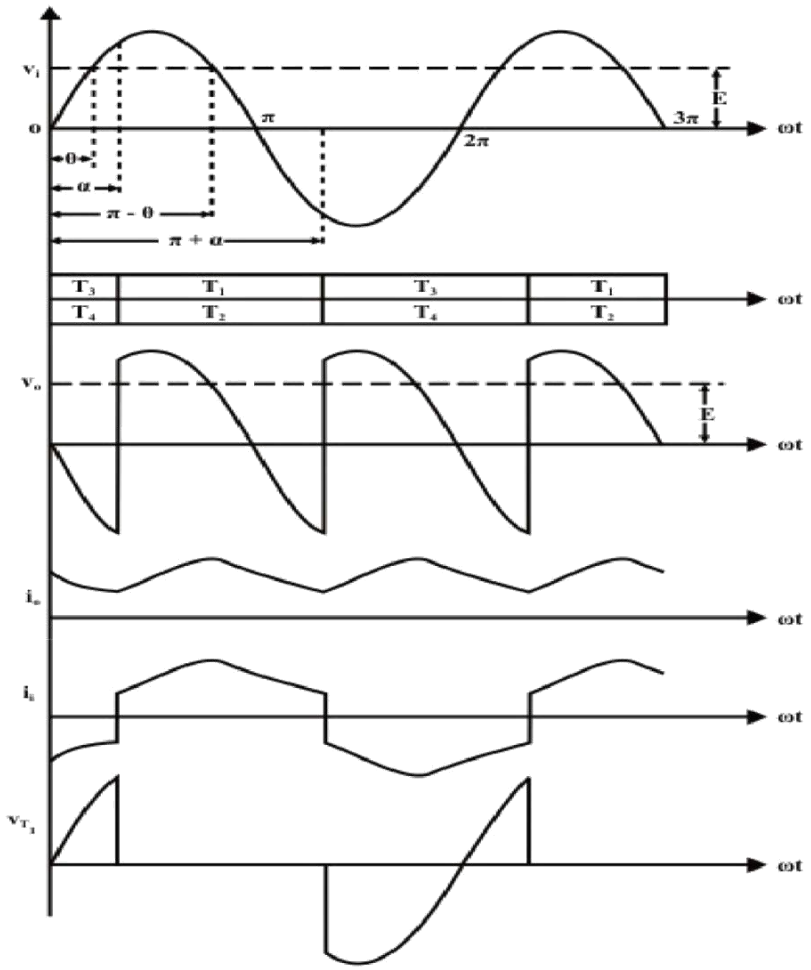


Fig. 10.4: Waveforms in Single phase fully controlled bridge convertor in continuous conduction mode.

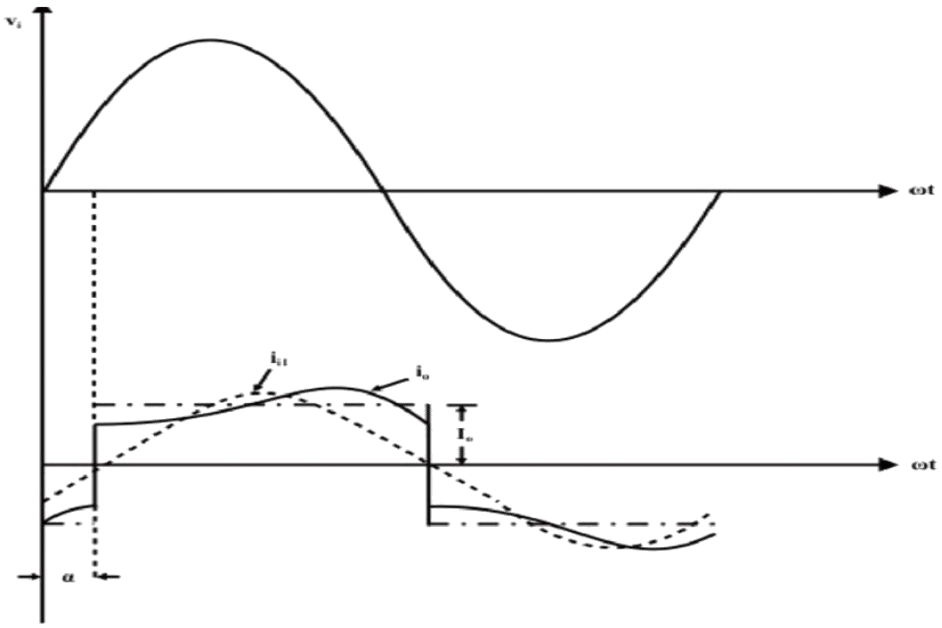


Fig. 10.5: The input current and its fundamental component

It will be of interest to find out a Fourier series expression of i_i. However, using actual expression for i_i will lead to exceedingly complex calculation. Significant simplification can be made by replacing i_0 with its average value I_0 . This will be justified provided the load is highly inductive and the ripple on i_0 is negligible compared to I_0. Under this assumption the idealized waveform of i_i becomes a square wave with transitions at t = and t = + as shown in Fig 10.5. i_{i1} is the fundantal component of this idealized i_i.

Evidently the input current displacement factor defined as the cosine of the angle between input voltage (v_i) and the fundamental component of input current (i_{i1}) waveforms is
cosα(lagging).

Therefore, the rectifier appears as a lagging power factor load to the input ac system. Larger the 'αpoorer is the power factor.

The input current i_i also contain significant amount of harmonic current (3rd, 5th, etc) and
therefore appears as a harmonic source to the utility. Exact composition of the harmonic currents
can be obtained by Fourier series analysis of i_i and is left as an exercise.

Fill in the blank(s) with the appropriate word(s).

i) A single phase fully controlled bridge converter can operate either in the _____ or _____ conduction mode.

ii) In the continuous conduction mode at least _____ thyristors conduct at all times.

iii) In the continuous conduction mode the output voltage waveform does not depend on the _____ parameters.

iv) The minimum frequency of the output voltage harmonic in a single phase fully controlled bridge converter is _____ the input supply frequency.

v) The input displacement factor of a single phase fully controlled bridge converter in the continuous conduction mode is equal to the cosine of the _____ angle.

Answer: (i) continuous, discontinuous; (ii) two; (iii) load; (iv) twice; (v) firing.

4.5 Operation in the discontinuous conduction mode

So far we have assumed that the converter operates in continuous conduction mode without paying attention to the load condition required for it. In figure 10.4 the voltage across the R and L component of the load is negative in the region - $\theta \leq t \leq +\pi$ Therefore i0 continues to decrease till a new pair of thyristor is fired at $t = +\pi$ Now if the value of R, L and E are such that i_0 becomes zero before $\omega t = \pi + \alpha$ the conduction becomes discontinuous. Obviously then, at the boundary between continuous and discontinuous conduction the minimum value of i_0 which occurs at t = and $t = +$ will be zero. Putting this condition in (10.26) we obtain the condition for continuous conduction as.

Fig 10.6 shows waveforms of different variables on the boundary between continuous and discontinuous conduction modes and in the discontinuous conduction mode. It should be stressed that on the boundary between continuous and discontinuous conduction modes the load current is still continuous. Therefore, all the analysis of continuous conduction mode applies to this case as well. However in the discontinuous conduction mode i_0 remains zero for certain interval. During this interval none of the thyristors conduct. These intervals are shown by hatched lines in the conduction diagram of Fig 10.6(b). In this conduction mode i_0 starts rising from zero as T_1T_2 are fired at t = . The load current continues to increase till t = - . After this, the output voltage v_0 falls below the emf E and i_0 decreases till t = when it becomes zero. Since the thyristors cannot conduct current in the reverse direction i_0 remains at zero till $\omega t = \pi + \alpha$ when T3 and T4 are fired. During the period t + none of the thyristors conduct. During this period v0 attains the value E.

Performance of the rectifier such as V_{OAV}, V_{ORMS}, I_{OAV}, I_{ORMS} etc can be found in termsof

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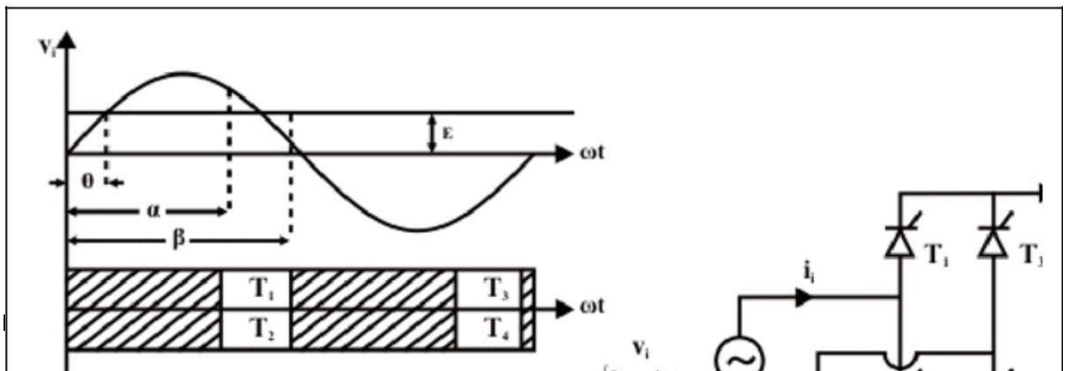


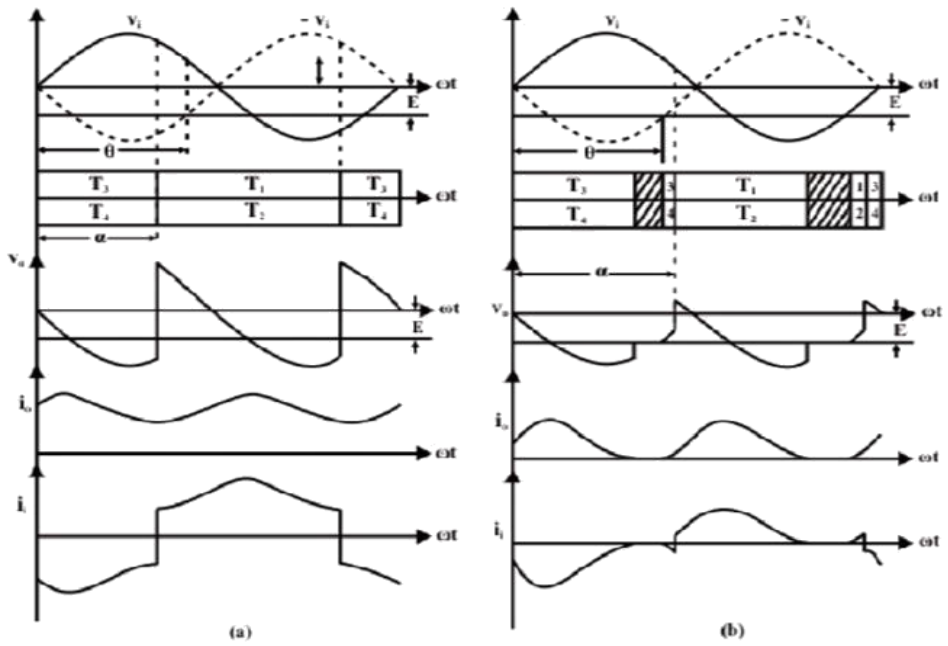


Fig. 10.8: Waveforms in the inverter mode of operation
(a) Continuous conduction;
(b) discontinuous conduction.

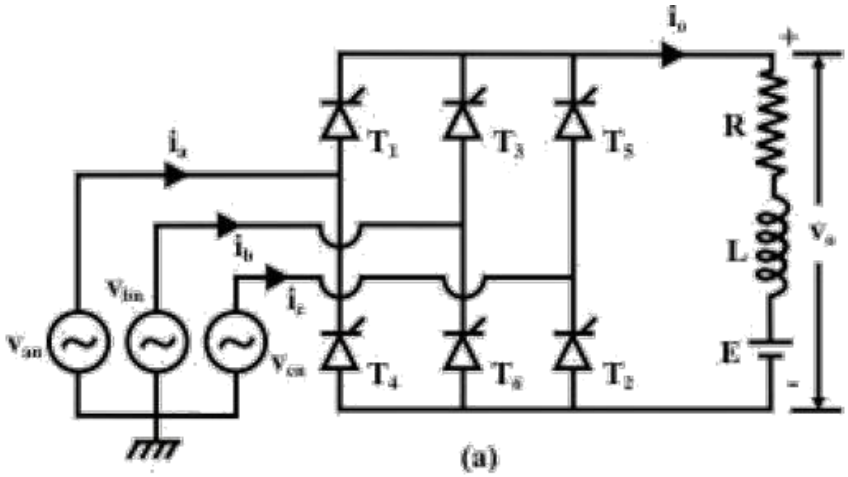
The three phase fully controlled bridge converter has been probably the most widely used power electronic converter in the medium to high power applications. Three phase circuits are preferable when large power is involved. The controlled rectifier can provide controllable out put dc voltage in a single unit instead of a three phase autotransformer and a diode bridge rectifier. The controlled rectifier is obtained by replacing the diodes of the uncontrolled rectifier with thyristors. Control over the output dc voltage is obtained by controlling the conduction interval of each thyristor. This method is known as phase control and converters are also called "phase controlled converters". Since thyristors can block voltage in both directions it is possible to reverse the polarity of the output dc voltage and hence feed power back to the ac supply from the dc side. Under such condition the converter is said to be operating in the "inverting mode". The thyristors in the converter circuit are commutated with the help of the supply voltage in the rectifying mode of operation and are known as "Line commutated converter". The same circuit while operating in the inverter mode requires load side counter emf. for commutation and are referred to as the "Load commutated inverter".

In phase controlled rectifiers though the output voltage can be varied continuously the load harmonic voltage increases considerably as the average value goes down. Of course the magnitude of harmonic voltage is lower in three phase converter compared to the single phase circuit. Since the frequency of the harmonic voltage is higher smaller load inductance leads to continuous conduction. Input current wave shape become rectangular and contain 5^{th} and higher order odd harmonics. The displacement angle of the input current increases with firing angle. The frequency of the harmonic voltage and current can be increased by increasing the pulse number of the converter which can be achieved by series and parallel connection of basic 6 pulse converters. The control circuit become considerably complicated and the use of coupling transformer and / or interphase reactors become mandatory.

With the introduction of high power IGBTs the three phase bridge converter has all but been replaced by dc link voltage source converters in the medium to moderately high power range. However in very high power application (such as HV dc transmission system, cycloconverter drives, load commutated inverter synchronous motor drives, static scherbius drives etc.) the basic B phase bridge converter block is still used. In this lesson the operating principle and characteristic of this very important converter topology will be discussed in source depth.

Operating principle of 3 phase fully controlled bridge converter

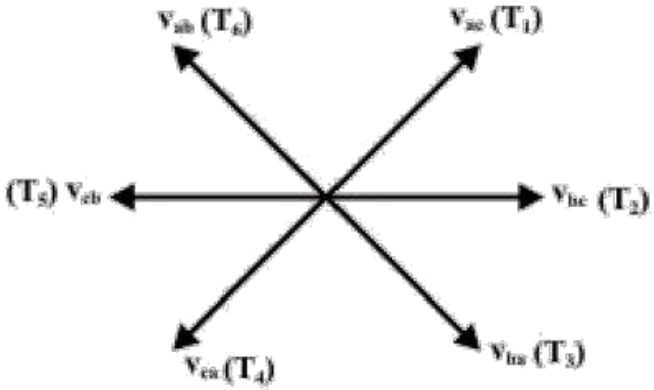
A three phase fully controlled converter is obtained by replacing all the six diodes of an uncontrolled converter by six thyristors as shown in Fig. 13.1 (a)



(a)

Device / Mode	V_{T1}	V_{T2}	V_{T3}	V_{T4}	V_{T5}	V_{T6}	V_o
T_1T_2	0	0	V_{ba}	V_{ca}	V_{ca}	V_{cb}	V_{ac}
T_2T_3	V_{ab}	0	0	V_{ca}	V_{cb}	V_{cb}	V_{bc}
T_3T_4	V_{ab}	V_{ac}	0	0	V_{cb}	V_{ab}	V_{ba}
T_4T_5	V_{ac}	V_{ac}	V_{bc}	0	0	V_{ab}	V_{ca}
T_5T_6	V_{ac}	V_{bc}	V_{bc}	V_{ba}	0	0	V_{cb}
T_6T_1	0	V_{bc}	V_{ba}	V_{ba}	V_{ca}	0	V_{ab}
NONE	-	-	-	-	-	-	E

(b)



(c)

Fig. 13.1: operation of a three phase full controlled bridge converter
(a) circuit diagram,
(b) conduction table,
(c) phaser diagram of line voltages.

For any current to flow in the load at least one device from the top group (T_1, T_3, T_5) and one from the bottom group (T_2, T_4, T_6) must conduct. It can be argued as in the case of an uncontrolled converter only one device from these two groups will conduct.

Then from symmetry consideration it can be argued that each thyristor conducts for 120° of the input cycle. Now the thyristors are fired in the sequence $T_1 \rightarrow T_2 \rightarrow T_3 \rightarrow T_4 \rightarrow T_5 \rightarrow T_6 \rightarrow T_1$ with 60° interval between each firing. Therefore thyristors on the same phase leg are fired at an interval of 180° and hence can not conduct simultaneously. This leaves only six possible conduction mode for the converter in the continuous conduction mode of operation. These are T_1T_2, T_2T_3, T_3T_4, T_4T_5, T_5T_6, T_6T_1. Each conduction mode is of 60° duration and appears in the sequence mentioned. The conduction table of Fig. 13.1 (b) shows voltage across different devices and the dc output voltage for each conduction interval. The phasor diagram of the line voltages appear in Fig. 13.1 (c). Each of these line voltages can be associated with the firing of a thyristor with the help of the conduction table-1. For example the thyristor T_1 is fired at the end of T_5 T_6 conduction interval. During this period the voltage across T_1 was v_{ac}. Therefore T_1 is fired α angle after the positive going zero crossing of v_{ac}. Similar observation can be made about other thyristors. The phasor diagram of Fig. 13.1 (c) also confirms that all the thyristors are fired in the correct sequence with 60° interval between each firing.

Fig. 13.2 shows the waveforms of different variables (shown in Fig. 13.1 (a)). To arrive at the waveforms it is necessary to draw the conduction diagram which shows the interval of conduction for each thyristor and can be drawn with the help of the phasor diagram of fig. 13.1 (c). If the converter firing angle is α each thyristor is fired "α" angle after the positive going zero crossing of the line voltage with which it's firing is associated. Once the conduction diagram is drawn all other voltage waveforms can be drawn from the line voltage waveforms and from the conduction table of fig. 13.1 (b). Similarly line currents can be drawn from the output current and the conduction diagram. It is clear from the waveforms that output voltage and current waveforms are periodic over one sixth of the input cycle. Therefore this converter is also called the "six pulse" converter. The input current on the other hand contains only odds harmonics of the input frequency other than the triplex (3^{rd}, 9^{th} etc.) harmonics. The next section will analyze the operation of this converter in more details.

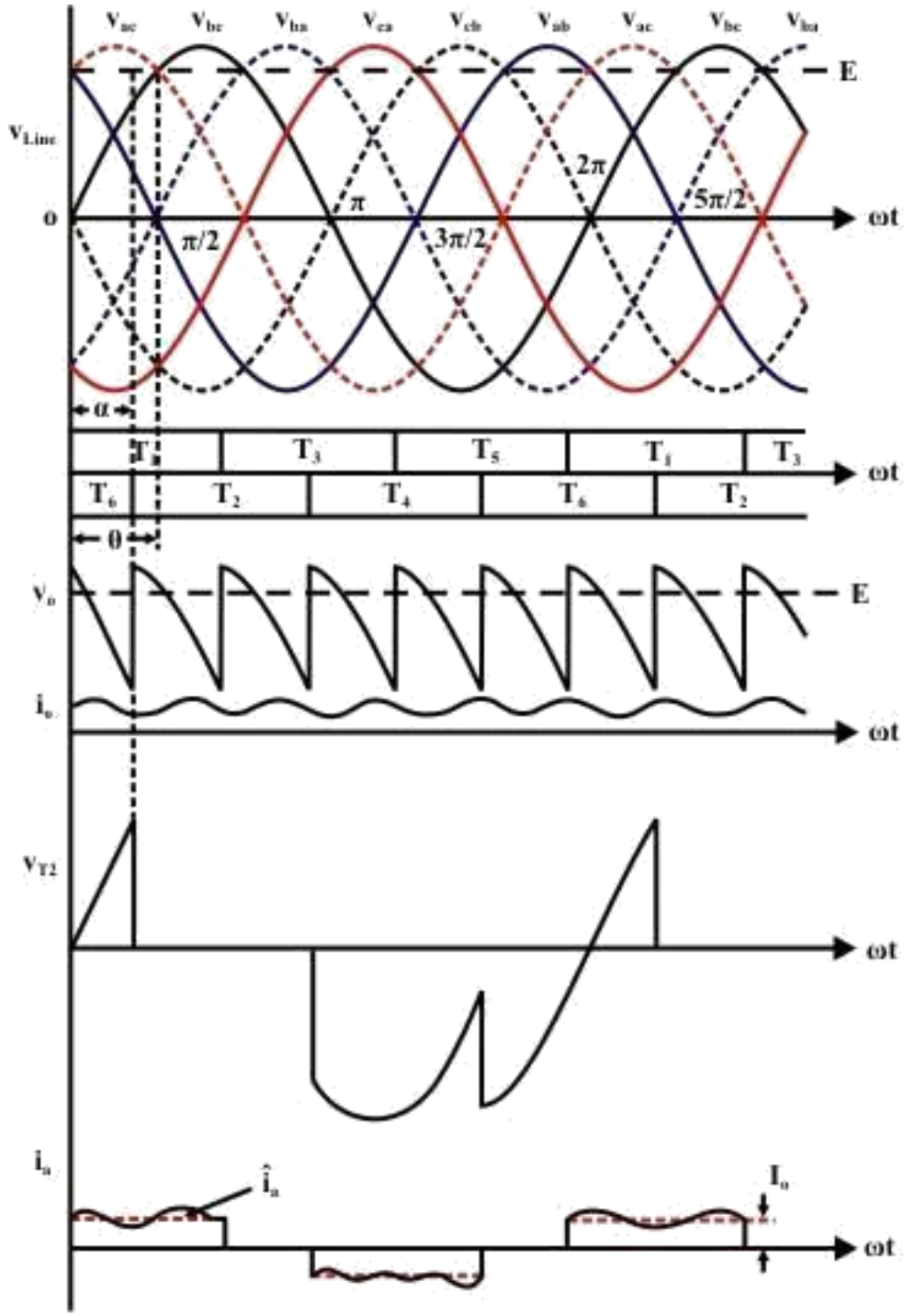


Fig. 13.2: Waveforms of three phase fully controlled converter 13.2.1 Analysis of the converter in the rectifier mode.

Analysis of the converter in the rectifier mode

The output voltage waveform can be written as

The input phase current i_a is expressed as

$$i_a = i_0 \qquad \alpha \le \omega t \le \alpha + \frac{\pi}{3}$$

$$i_a = -i_0 \qquad \alpha + \frac{2\pi}{3} \le \omega t \le \alpha + \frac{4\pi}{3}$$

$$i_a = i_0 \qquad \alpha + \frac{5\pi}{3} \le \omega t \le \alpha + 2\pi$$

$$i_a = 0 \qquad \text{otherwise}$$

From Fig. 13.2 it can be observed that i_0 itself has a ripple at a frequency six times the input frequency. The closed from expression of i_0, as will be seen later is some what complicated. However, considerable simplification in the expression of i_a can be obtained if i_0 is replaced by its average value I_0. This approximation will be valid provided the ripple on i_0 is small, i.e, the load is highly inductive. The modified input current waveform will then be i_a which can be expressed in terms of a fourier series as

To find out the condition for continuous conduction it is noted that in the limiting case of continuous conduction.

$$i_{0\,\min} = 0 \text{ at } \omega t = \alpha + \frac{\pi}{3}, \text{ Now if } \theta \le \alpha + \frac{\pi}{3} \text{ then } i_0 \text{ is minimum at } \omega t = \alpha. \therefore \text{Condition}$$

for continuous conduction is $i_0 \big|_{\omega t=\alpha} \ge 0$. However discontinuous conduction is rare in these conversions and will not be discussed any further.

Analysis of the converter in the inverting mode.

In all the analysis presented so far it has been assumed that $\alpha < 90°$. It follows from equation 13.2 that the output dc voltage will be positive in this case and power will be flowing from the three phase ac side to the dc side. This is the rectifier mode of operation of the converter. However if α is made larger than 90° the direction of power flow through the converter will reverse provided there exists a power source in the dc side of suitable polarity. The converter in that case is said to be operating in the inverter mode. It has been explained in connection with single phase converters that the polarity of EMF source on the dc side [Fig. 13.1(a)] would have to be reversed for inverter mode of operator. Fig. 13.3 shows the circuit connection and wave forms in the inverting mode of operation where the load current has been assumed to be continuous and ripple free.

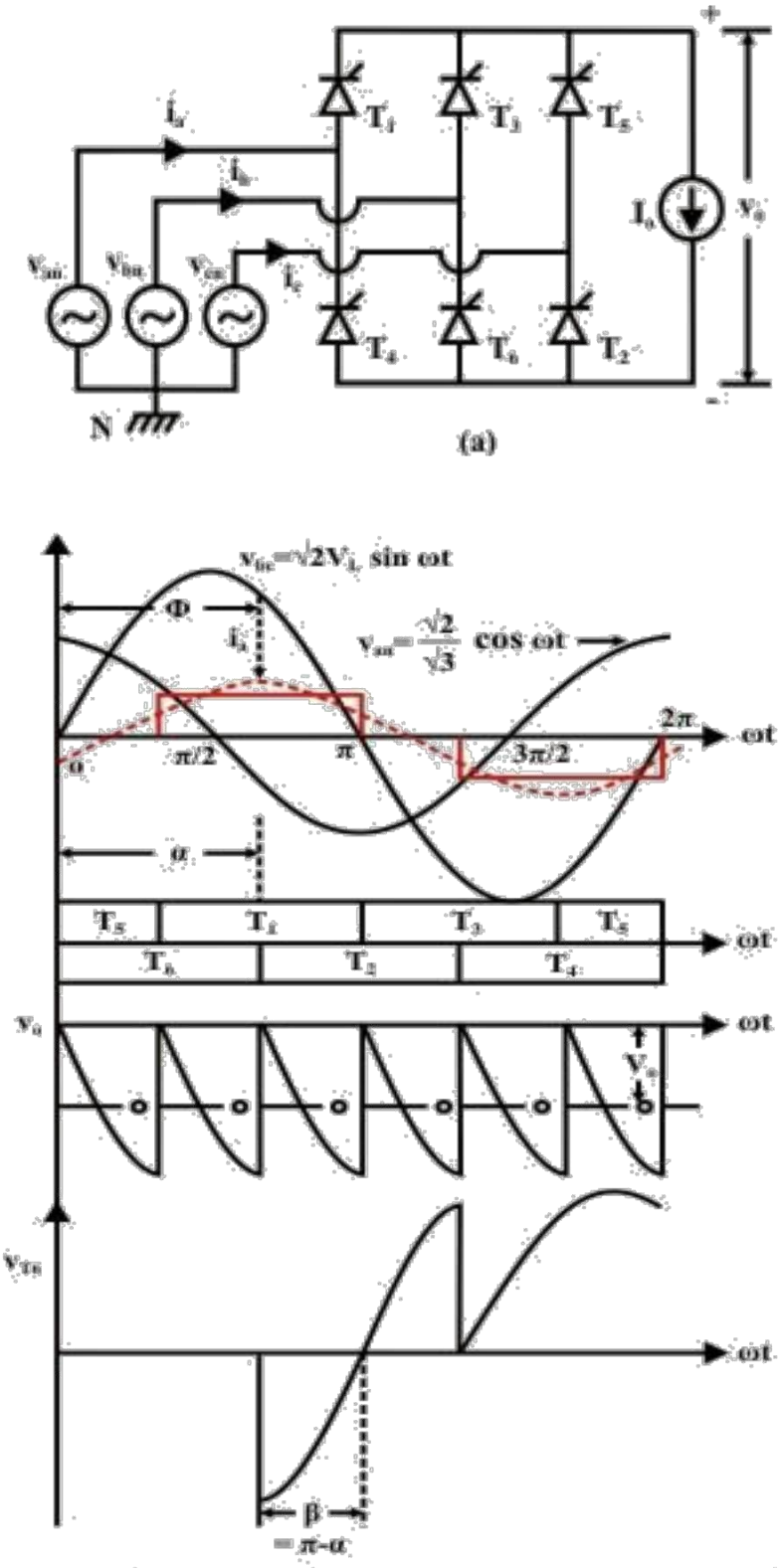


Fig. 13.3(b): Inverter mode of operation of the three phase fully controlled bridge converter
(a) circuit diagram
(b) waveforms.

Analysis of the converter in the inverting mode is similar to its rectifier mode of operation. The same expressions hold for the dc and harmonic compounds in the output voltage and current. The input supply current Fourier series is also identical to Equation 13.8. In particular

$$V_0 = \frac{3\sqrt{2}}{\pi} V_L \cos\alpha \qquad (13.24)$$

$$i_{a1} = \frac{2\sqrt{3}}{\pi} I_0 \cos(\omega t - \alpha) \qquad (13.25)$$

For values of α in the range 90° < α < 180° it is observed from Fig. 13.3(b) that the average dc voltage is negative and the displacement angle φ of the fundamental component of the input ac line current is equal to α > 90°. Therefore, power in the ac side flows from the converter to the source.

It is observed form Fig. 13.3(b) that an outgoing thyristor (thyristor T_6 in Fig. 13.3(b)) after commutation is impressed with a negative voltage of duration β = π – α. For successful commutation of the outgoing thyristor it is essential that this interval is larger than the turn off time of the thyristor i.e,

$\beta \geq \omega t_q$, t_q is the thyristor turn off time

Therefore $\pi - \alpha \geq \omega t_q$ or $\alpha \leq \pi - \omega t_q$.

Which imposes an upper limit on the value of α. In practice this upper value of α is further reduced due to commutation overlap.

Exercise 13.2

A three phase fully controlled bridge converter operating from a 3 phase 220 V, 50 Hz supply is used to charge a battery bank with nominal voltage of 240 V. The battery bank has an internal resistance of 0.01 Ω and the battery bank voltage varies by ± 10% around its nominal value between fully charged and uncharged condition. Assuming continuous conduction find out.

- The range of firing angle of the converter.
- The range of ac input power factor.
- The range of charging efficiency.

When the battery bank is charged with a constant average charging current of 100 Amps through a 250 mH lossless inductor.

Answer: The maximum and minimum battery voltages are, $V_{B\ Min} = 0.9 \times V_{B\ Nom} = 216$ volts and $V_{B\ Max} = 1.1 \times V_{B\ Nom} = 264$ volts respectively.

Since the average charging current is constant at 100 A.

$V_{0\ Max} = V_{B\ Max} + 100 \times R_B = 264 + 100 \times 0.01 = 265$ volts
$V_{0\ Min} = V_{B\ Min} + 100 \times R_B = 216 + 100 \times 0.01 = 217$ volts.

2. A three phase fully controlled converter operates from a 3 phase 230 V, 50 Hz supply through a Y/ transformer to supply a 220 V, 600 rpm, 500 A separately excited dc motor. The motor has an armature resistance of 0.02 Ω. What should be the transformer turns ratio such that the converter produces rated motor terminal voltage at 0º firing angle. Assume continuous conduction. The same converter is now used to brake the motor regeneratively in the reverse direction. If the thyristors are to be provided with a minimum turn off time of 100 μs, what is the maximum reverse speed at which rated braking torque can be produced.

Answer: From the given question

$$\frac{3\sqrt{2}}{\pi} V = 220 \qquad \therefore V_L = 162.9\ V$$

Where V_L is the secondary side line and also the phase voltage since the secondary side is connected.

Primary side phase voltage = $\frac{230}{\sqrt{3}} V = 132.79$ V

$\therefore$ Turns ratio = $^{132}_{162} : ^{79}_{9} = 1:1.2267$.

During regenerative braking in the reverse direction the converter operates in the inverting mode.

$tq|_{Min} = 100 \mu S \qquad \therefore \beta_{Min} = \omega tq_{Min} = 1.8^o$

6 $\alpha_{Max} = 180 - \beta_{Min} = 178.2^o$

7 Maximum negative voltage that can be generated by the converter is

$$\frac{3\sqrt{2}}{\pi} V_L \cos 178.2^o = -219.89$$

V For rated braking torque $I_a = 500$ A

$\therefore E_b = V_a - I_a r_a = -229.89$ V.

At 600 RPM $E_b = 220 - 500 \times 0.02 = 210$ V.

∴ Max reverse speed is $\frac{229.89}{210} \times 600 = 656.83$ RPM .

Higher pulse number converters and dual converter

The three phase fully controlled converter is widely used in the medium to moderately high power applications. However in very large power applications (such as HV DC transmission systems) the device ratings become impractically large. Also the relatively low frequency (6^{th} in the dc side, 5^{th} and 7^{th} in the ac side) harmonic voltages and currents produced by this converter become unacceptable. Therefore several such converters are connected in series parallel combination in order to increase the voltage / current rating of the resulting converter. Furthermore if the component converters are controlled properly some lower order harmonics can be eliminated both from the input and output resulting in a higher pulse converter.

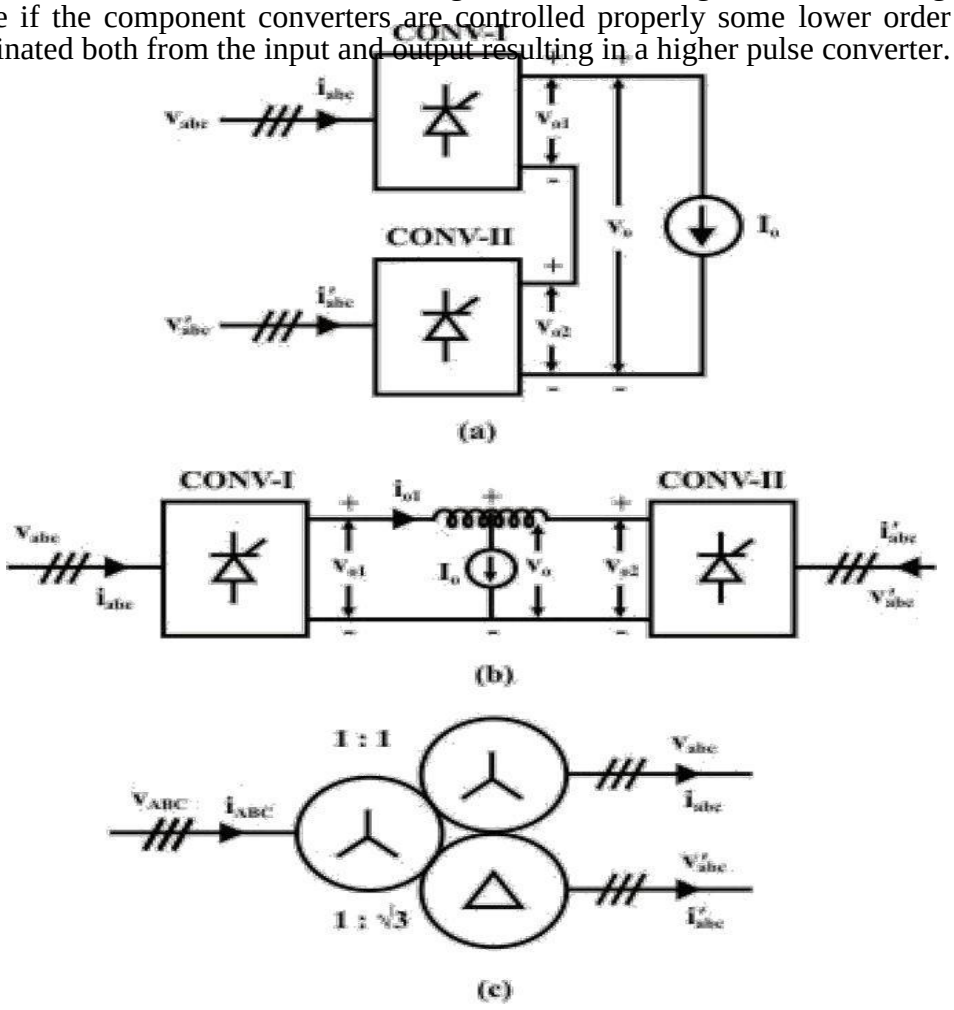


Fig. 13.4: Series and parallel connection of 6 phase converters
(a) Series connection,
(b) parallel connection,
(c) Transformer connection.

Fig. 13.4(a) schematically represents series connection of two six pulse converters where as Fig. 13.4(b) can be considered to be a parallel connection. The inductance in between the converters has been included to limit circulating harmonic current. In both these figures CONV – I and CONV – II have identical construction and are also fired at the same firing angle α. Their input supplies also have same magnitude but displaced in phase by an angle φ. Then one can write

Now if cos 3Kφ = 0 for some K then the corresponding harmonic disappear from the fourier series expression of v_0.

In particular if φ = 30° then cos 3Kφ = 0 for K = 1, 2, 3, 5…….
This phase difference can be obtained by the arrangement shown in Fig.

13.4(c). Then

It can be seen that the frequency of the harmonics present in the output voltage has the form

12ω, 24ω, 36ω ……..

Similarly it can be shown that the input side line current i_{ABC} have harmonic frequency of the form

11ω, 13ω, 23ω, 25ω, 35ω, 37ω, …….

Which is the characteristic of a 12 pulse converter.

In a similar manner more number of 3 phase 6 pulse converters can be connected in series / parallel and the φ angle can be adjusted to obtain 18 and 24 pulse converters.

One of the shortcomings of a three phase fully controlled converter is that although it can produce both positive and negative voltage it can not supply current in both directions. However, some applications such as a four quadrant dc motor drive require this capability from the dc source. This problem is easily mitigated by connecting another three phase fully controlled converter in anti parallel as shown in Fig. 13.5 (a). In this figure converter -I supplies positive load current while converter-II supplies negative load current. In other words converter-I operates in the first and fourth quadrant of the output v – i plane whereas converter-II operates in the third and fourth quadrant. Thus the two converters taken together can operate in all four quadrants and is capable of supplying a four quadrant dc motor drive. The combined converter is called the Dual converter.

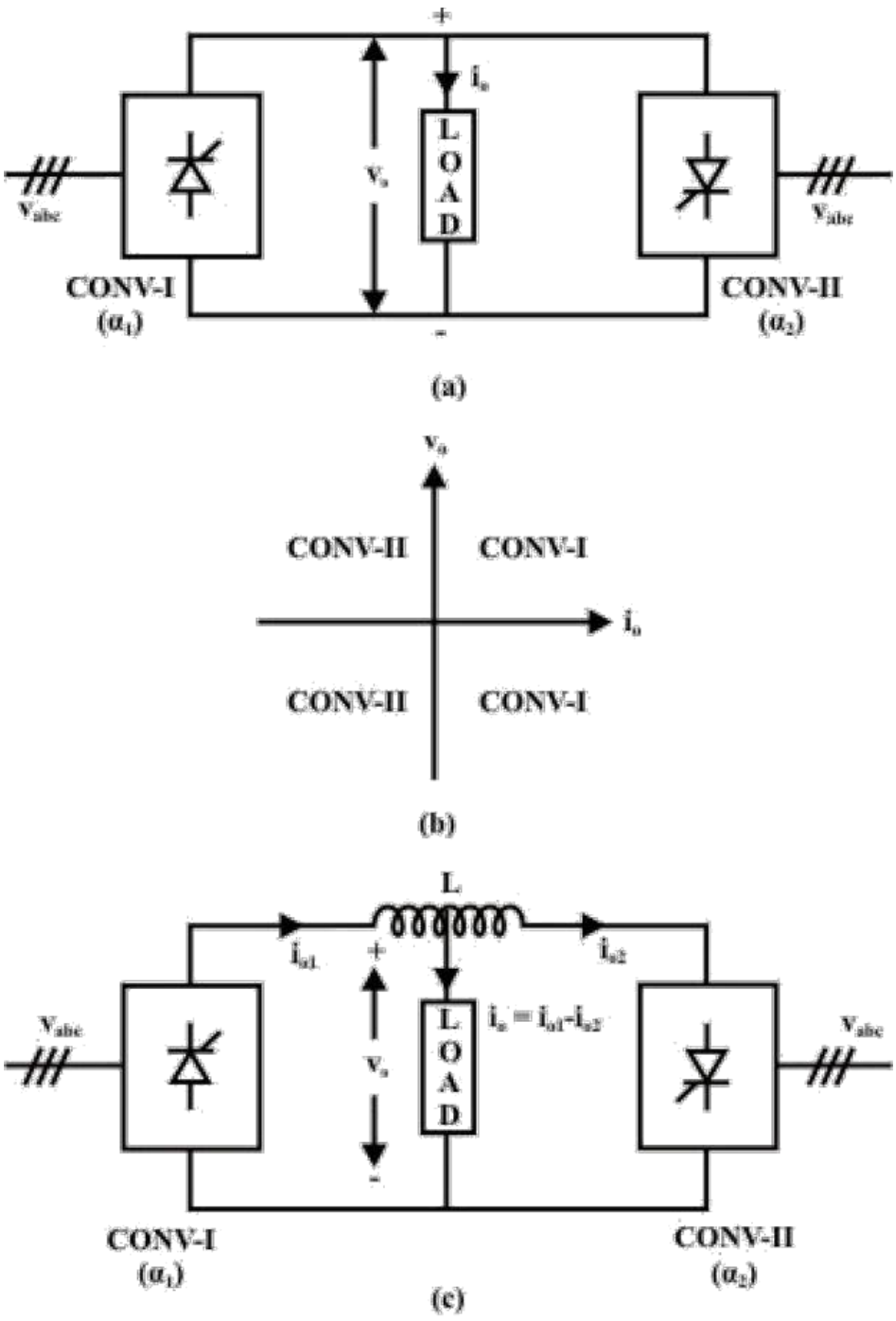


Fig. 13.5: Dual converter circuits
(a) non circulating type
(b) output V-I plane
(c) circulating current type

Obviously since converter-I and converter-II are connected in antiparallel they must produce the same dc voltage. This requires that the firing angles of these two converters be related as

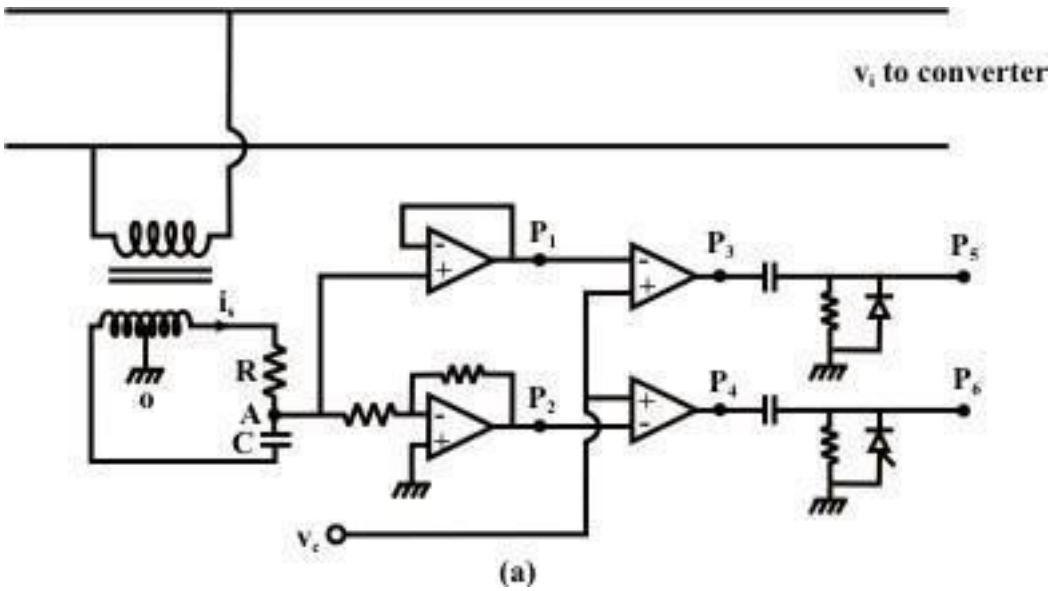
$$\alpha_2 = \pi - \alpha_1 \qquad (13.30)$$

Although Equations 13.30 ensures that the dc voltages produced by these converters are equal the output voltages do not match on an instantaneous basis. Therefore to avoid a direct short circuit between two different supply lines the two converters must never be gated simultaneously. Converter-I receives gate pulses when the load current is positive. Gate pulses to converter-II are blocked at that time. For negative load current converter-II thyristors are fired while converter-I gate pulses are blocked. Thus there is no circulating current flowing through the converters and therefore it is called the non-circulating current type dual converter. It requires precise sensing of the zero crossing of the output current which may pose a problem particularly at light load due to possible discontinuous conduction. To overcome this problem an interphase reactor may be incorporated between the two converters. With the interphase reactor in place both the converters can be gated simultaneously with $\alpha_2 = \pi - \alpha_1$. The resulting converter is called the circulating current type dual converter.

Gate Drive circuit for three phase fully controlled converter

Several schemes exist to generate gate drive pulses for single phase or three phase converters. In many application it is required that the output of the converter be proportional to a control voltage. This can be achieved as follows.

The following circuit can be used to generate "α" according to equation 13.32.



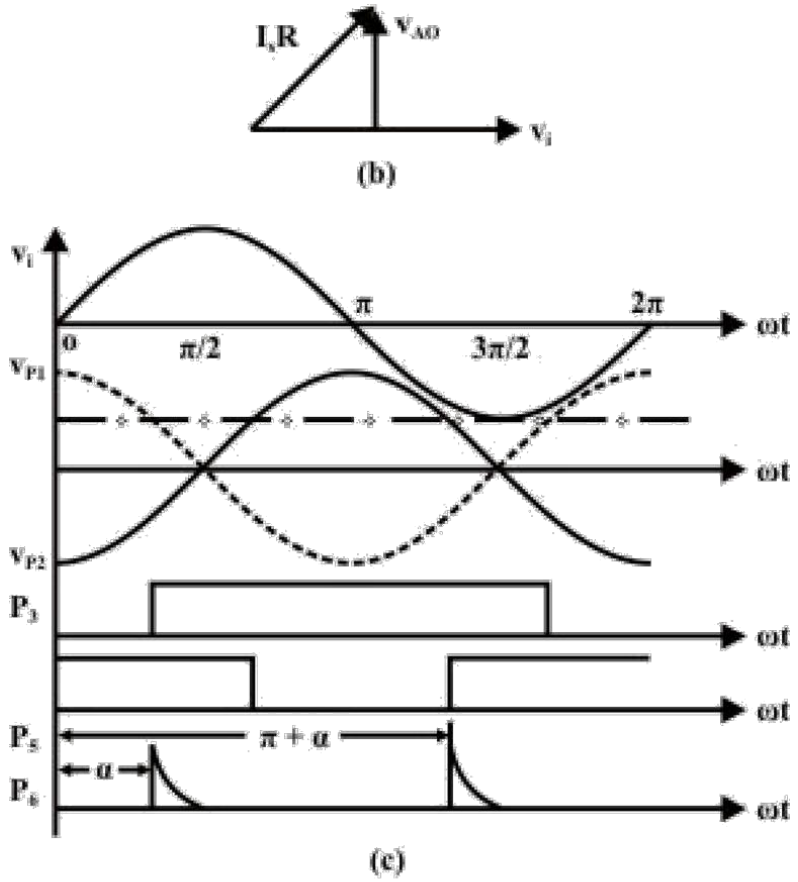
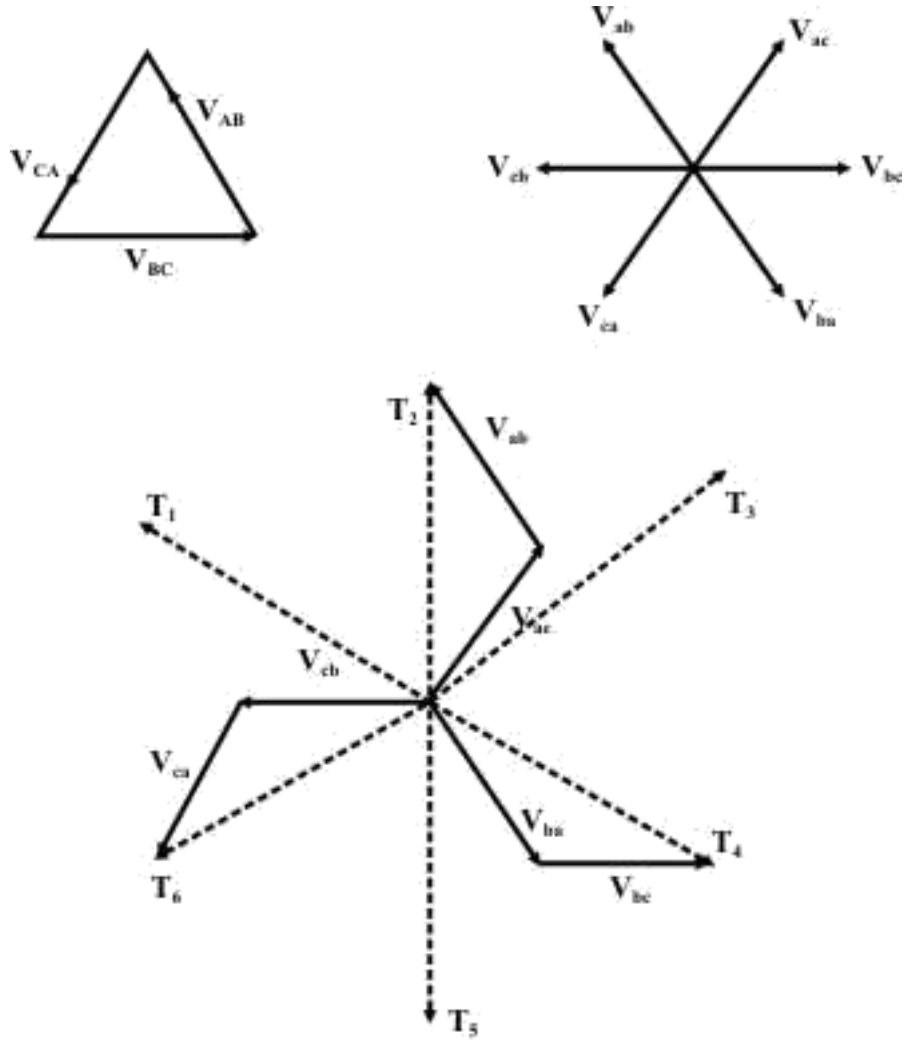


Fig. 13.6: Triggering circuit for single phase converter
(a) circuit diagram
(b) phasor diagram
(c) waveforms

In the circuit of Fig. 13.6(a) a phase shift network is used to obtain a waveform leading v_i by 90º. The phasor diagram of the phase shift circuit is shown in Fig. 13.6(b). The output of the phase shift waveform (and its inverse) is compared with v_C. The firing pulse is generated at the point when these two waveforms are equal. Obviously at-this instant

Therefore this method of generation of converter firing pulses is called "inverse cosine" control.
The output of the phase shift network is called carrier waveform.

Similar technique can be used for three phase converters. However the phase shift network here consists of a three phase signal transformer with special connections as shown in Fig. 13.7.



(b)

Fig. 13.7: Carrier wave generation three phase converters
(a) Transformer connection
(b) phasor diagram.

The signal transformer uses three single phase transformer each of which has two secondary windings. The primary windings are connected in delta while the secondary windings are connected in zigzag. From Fig. 13.1 (c) T_2 is fired α angle after the positive going zero crossing of v_{bc}. Therefore, to implement inverse cosine the carrier wave for T_2 must lead v_{bc} by 90º. This waveform is obtained from zigzag connection of the winding segments a_1a_2 and c_1c_2 as shown in Fig. 13.7(a). The same figure also shows the zigzag connection for other phase. The voltage across each zigzag phase can be used to fire two thyristors belonging to the same phase leg using a circuit similar to Fig. 13.6 (a). The phase shift network will not be required in this case.

Exercise 5.3

1. Fill in the blank(s) with the appropriate word(s)

   i) Higher pulse number converters can be realized by _____ and _____ connection of six pulse converters.

   ii) Constituent six pulse converters of a 12 pulse converter have _____ firing angles.

   iii) The input supply voltages to the converters of a 12 pulse converter have _____ magnitudes and are phase shifted from one another by _____ degrees.

   iv) The input supply to a 12 pulse converter can be obtained through a _____ connected transformer.

   v) Dual converters are used for supplying _____ quadrant dc motor drives.

   vi) In a dual converter if one converter is fired at an angle 'α' the other has to be fired at _____.

   vii) In _____ current dual converter only one converter conducts t any time.

   viii) In a circulating current type dual converter an _____ is used between the converters to limit the circulating current.

   ix) To obtain a linear control relation between the control voltage and the output dc voltage of a converter _____ control logic is used.

   x) In a three phase fully controlled converter the carrier waves for firing pulse generation are obtained using three _____ connected single phase transformers.

Answers: (i) Series, parallel; (ii) same, (iii) equal, 30, (iv) star – star – delta; (v) four; (vi) π - α, (vii) non-circulating ; (viii) inductor, (ix) inverse-cosine; (x) delta-zigzag.

3. What will happen if the signal transformers generating the carrier wave have delta – double star connection instead of delta-zigzag connection.

Answer: With delta-double star connection of the signal transformers the carrier wave forms will be in phase with the line voltage waveforms. Therefore, without a phase shift network it will not be possible to generate carrier waveforms which are in quadrature with the line voltages. Hence inverse casine control law cannot be implemented.

Summary

- A three phase fully controlled converter is realized by replacing the diodes of an uncontrolled converter with thyristors.
- A three phase fully controlled converter can operate either as a rectifier or as an inverter.
- The output voltage of a three phase fully controlled converter contains multiple of sixth

harmonic of the input frequency in addition to the dc component.

- The input current of a three phase fully controlled converter contains only odd harmonics other than tripler harmonics.
- The input current displacement factor of a three phase fully controlled converter is cos α. α being the firing angle.
- In the continuous conduction mode a three phase fully controlled converter may operate in the inverting mode by increasing α beyond 90º.
- In the inverting mode the firing angle should be less than 180º for safe commutation of the thyristors.
- Several units of three phase fully controlled converters can be connected in series parallel to form higher pulse number (12, 18, 24 etc) converters.
- In higher pulse number converters all component converters are fired at the same firing angle while their input supplies are phase shifted from one another by a predetermined angle.
- Two three phase fully controlled converter can be connected in anti parallel to form a dual converter which can operate in all four quadrants of the V-I plane.
- Dual converters can be of circulating and non circulating current type.
- Fully controlled converters employ "inverse casine control" strategy for generating firing pulses which gives linear relationship between the output voltage and the control voltage. In a three phase fully controlled converter, a three phase delta/zig-zag connected signal transformer is used to generate the required carrier waves for this purpose.

.

AC to AC voltage converters operates on the AC mains essentially to regulate the output voltage. Portions of the supply sinusoid appear at the load while the semiconductor switches block the remaining portions. Several topologies have emerged along with voltage regulation methods, most of which are linked to the development of the semiconductor devices.

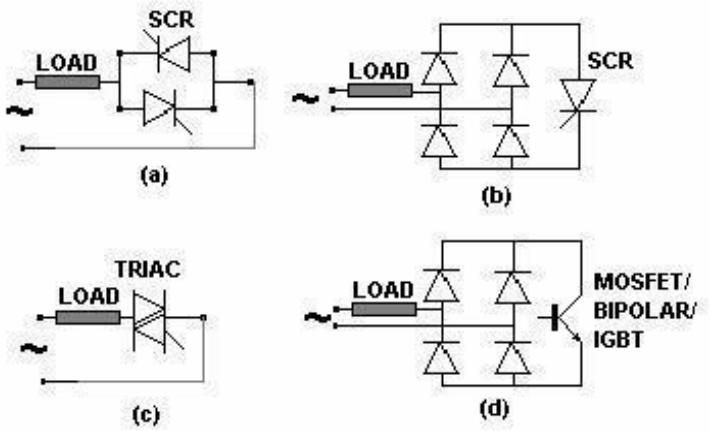


Fig 26.1 Some single phase AC-AC voltage regulator topologies. (a) Back-to -back SCR; (b) One SCR in (a) replaced by a four-diode full wave diode bridge; (c) A bi-directionally conducting TRIAC; (d) The SCR in (b) replaced by a transistor.

The regulators in Fig 26.1 (a), (b) and (c) perform quite similarly. They are called Phase Angle Controlled (PAC) AC-AC converters or AC-AC choppers. The TRIAC based converter may be considered as the basic topology. Being bi-directionally conducting devices, they act on both polarities of the applied voltage. However, $dv/dt_{re\ -applied}$ their ratings being poor, they tend to turn-on in the opposite direction just subsequent to their turn-off with an inductive load. The 'Alternistor' was developed with improved features but was not popular. The TRIAC is common only at the low power ranges. The (a) and (b) options are improvements on (c) mostly regarding current handling and turn-off-able current rating.

A transistorised AC-AC regulator is a PWM regulator similar to the DC-DC converters. It also requires a freewheeling path across the inductive load, which has also got to be bi-directional. Consequently, only controlled freewheeling devices can be used.

26.2 Operation with resistive loads

Fig. 26.2 illustrates the operation of the PAC converter with a resistive load. The device(s) is triggered at a phase-angle 'α' in each cycle. The current follows the voltage wave shape in each half and extinguishes itself at the zero crossings of the supply voltage. In the two-SCR topology, one SCR is positively biased in each half of the supply voltage. There is no scope for conduction overlap of the devices. A single pulse is sufficient to trigger the controlled devices with a resistive load. In the diode-SCR topology, two diodes are forward biased in each half. The SCR always receives a DC voltage and does not distinguish the polarity of the supply. It is thus always forward biased. The bi-directional TRIAC is also forward biased for both polarities of the supply voltage.

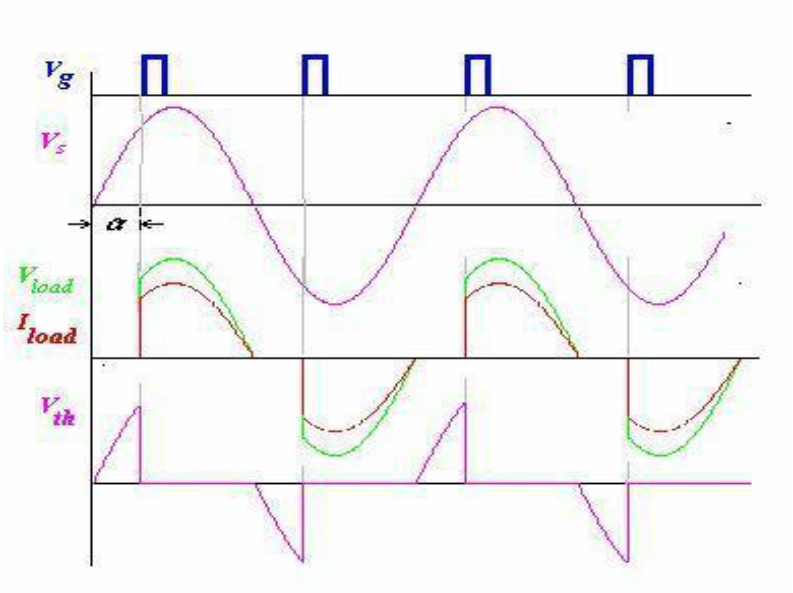


Fig. 26.2 Operation of a Phase Angle Controlled AC-AC converter with a resistive load

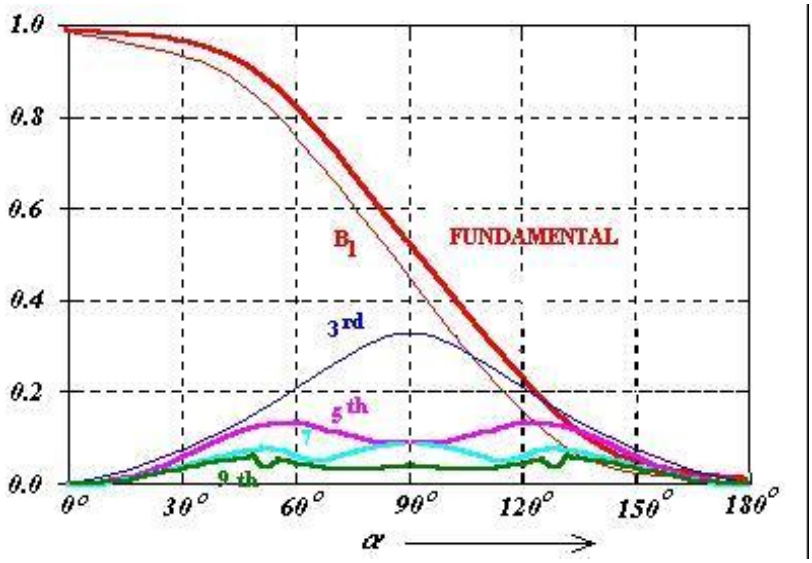


Fig. 26.3 The rms output voltage and the most important harmonics versus triggering angle α.

As is evident from the current waveforms, the PAC introduces significant harmonics both into the load and the supply. This is one of the main reasons why such controllers are today not acceptable. The ideal waveform as shown in Fig 26.2 is half wave symmetric. However it is to be achieved by the trigger circuits. The controller in Fig. 26.4 ensures this for the TRIAC based circuit. While the TRIAC has a differing characteristic for the two polarities of biasing with the 32V DIAC - a two terminal device- triggering is effected when the capacitor voltage reaches 32 V. This ensures elimination of DC and even components in the output voltage.

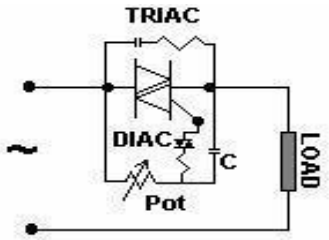


Fig. 26.4 DIAC based trigger circuit for a TRIAC to ensure symmetrical triggering in the two halves of the supply.

For the SCR based controllers, identical comparators for the two halves of the AC supply, which generates pulses for the two SCRs ensures DC and even harmonic free operation.

The PAC operates with a resistive load for all values of α ranging from 0^o **The fundamental current,** i_f can be represented as

In machine drives it is only the fundamental component, which is useful. However, in resistance heating type of application all harmonics are of no consequence. The corrupted supply current nevertheless is undesirable.

The power factor of a nonlinear deserves a special discussion. Fig. 26.2 shows the supply voltage and the non-sinusoidal load current. The fundamental load/supply current lags the supply voltage by the φ1, 'Fundamental Power Factor' angle. Cosφ1 is also called the 'Displacement Factor'. However this does not account for the total reactive power drawn by the system. This power factor is inspite of the actual load being resistive! The reactive power is drawn also y the trigger-angle dependent harmonics. Now

The portion within square brackets in Eq. 26.5 is identical to the first part of the expression within brackets in Eq. 26.1, which is called the Fourier coefficient 'B_1B'. The rms load voltage can also be similarly obtained by integrating between α and π and the result can be combined with Eq. 26.5 to give

$$power\ \ factor = per-unit\ \ rms\ \ load-current$$

$$= \sqrt{per-unit\ \ load\ \ power}$$

$$= \sqrt{B\ \ p.u.}$$

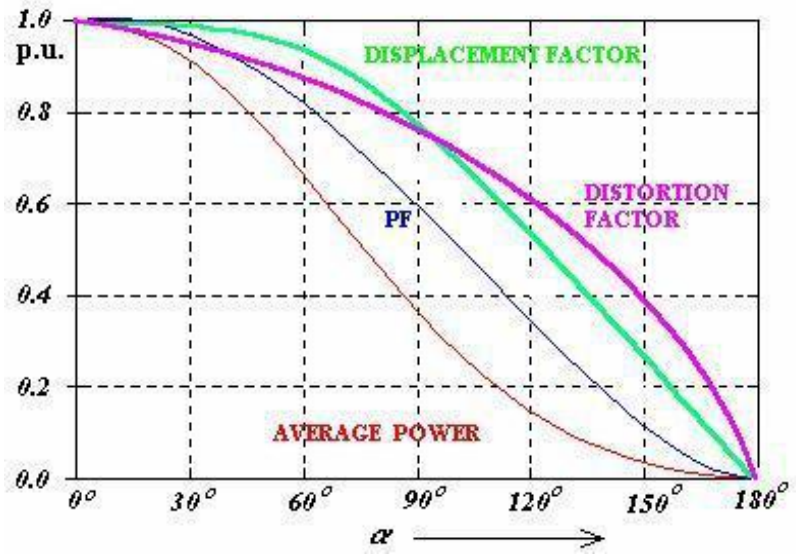


Fig. 26.5 Variation of various performance parameters with triggering angle

Operation with inductive loads

With inductive loads the operation of the PAC is illustrated in Fig 26.5. The current builds up from zero in each cycle. It quenches not at the zero crossing of the applied voltage as with the resistive load but after that instant. The supply voltage thus continues to be impressed on the load till the load current returns to zero. A single-pulse trigger for the TRIAC 26.1 (c) or the anti-parallel SCR (b) has no effect on the devices if it (or the anti-parallel device) is already in conduction in the reverse direction. The devices would fail to conduct when they are intended to, as they do not have the supply voltage forward biasing them when the trigger pulse arrives. A single pulse trigger will work till the trigger angle $\alpha > \varphi$, where φ is the power factor angle of the inductive load. A train of pulses is required here. The output voltage is controllable only between triggering angles φ and 180^{o}.

The load current waveform is further explained in Fig. 26.6. The current is composed of two components. The first is the steady state component of the load current, i_{ss} and the second, i_{tr} is the transient component.

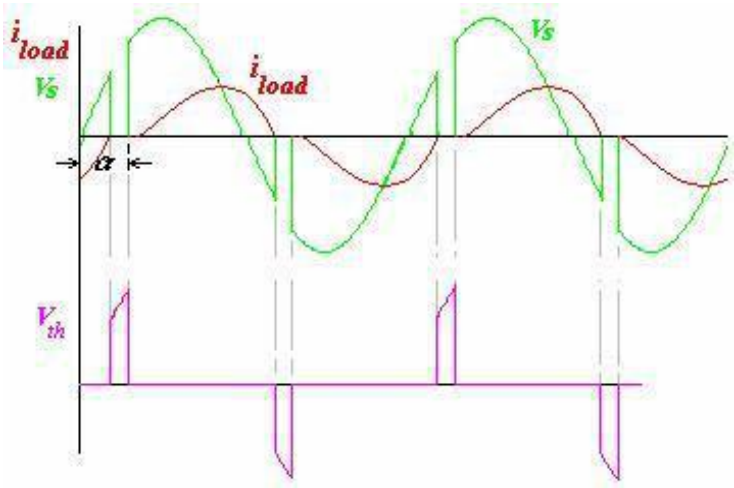


Fig. 26.6 Operation of a single phase PAC with an inductive load

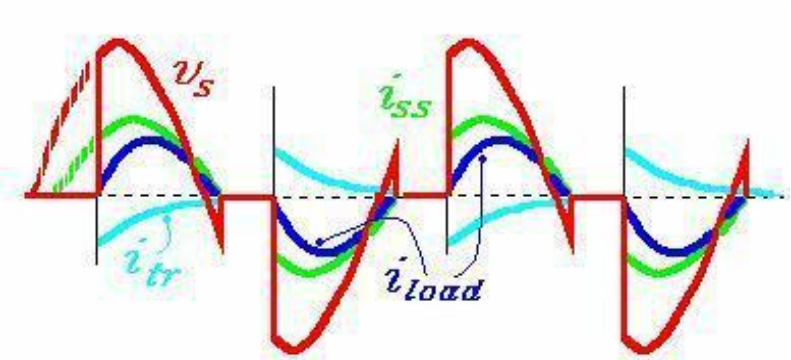


Fig 26.7 Load current for a single phase AC-AC converter with a R_L load. V_S - supply voltage, i_{ss} -steady state current component , i_{tr} - transient current component and i_{load} - load current ($= i_{ss} + i_{tr}$).

With an inductance in the load the distinguishing feature of the load current is that it must always start from zero. However, if the switch could have permanently kept the load connected to the supply the current would have become a sinusoidal one phase shifted from the voltage by the phase angle of the load, φ. This current restricted to the half periods of conduction is called the 'steady-state component' of load current i_{ss}. The 'transient component' of load current i_{tr}, again in each half cycle, must add up to zero with this i_{ss} to start from zero. This condition sets the initial value of the transient component to that of the steady state at the instant that the SCR/TRIAC is triggered. Fig. 26.6 illustrates these relations.

When a device is in conduction, the load current is governed by the equation

$$L\, di/dt + Ri = v_s$$

$$i_{load} = \frac{\sqrt{2}V}{Z}[\sin(\omega t - \varphi) + \sin(\alpha - \varphi)e^{\frac{-R}{L}(\alpha\omega - t)}] - /$$

Since at $t = 0$, $i_{load} = 0$ and supply voltage $v_s = \sqrt{2}V\sin\omega t$ the solution is of the form

The instant when the load current extinguishes is called the extinction angle β. It can be inferred that there would be no transients in the load current if the devices are triggered at the power factor angle of the load. The load current I that case is perfectly sinusoidal.

26.5 AC-AC Chopper

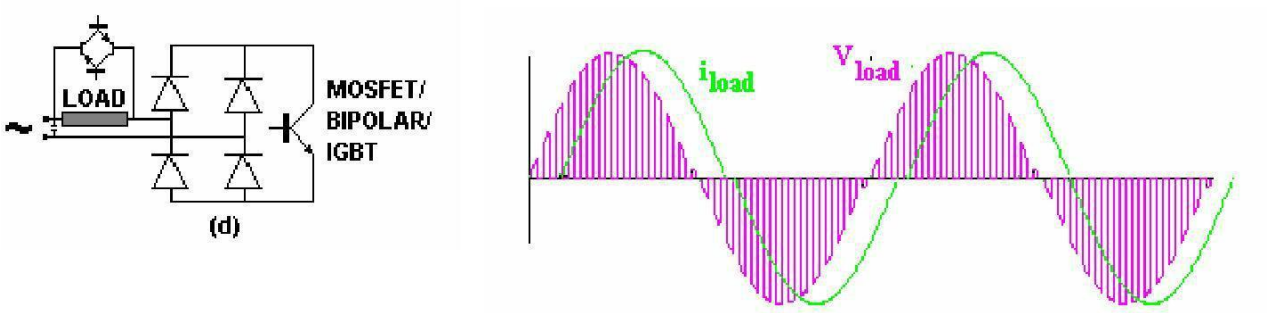


Fig. 26.8 A complete Transitorised AC-AC chopper topology of the version shown in Fig. 26.1 and the corresponding load voltage and current waveforms for an inductive load. The output voltage is shown to be about 50% for a 0.5 Duty Ratio chopping.

The AC-AC converter shown in Fig 26.1 has to be augmented with two additional controlled devices clamping the load as indicated in Fig. 26.7. A large capacitor across the supply terminals is also to be inserted. These devices which are mostly transistors of the same variety as used for the chopper are necessary to clamp the voltages generated by the switching-off of the current carrying inductors in the load while the input capacitor takes care of the line inductances. The harmonics in the line current and load voltage waveforms are significantly different from those with the PACs. Mostly switching frequency harmonics are present in both the waveforms.

PAC as a static switch

Both single phase and three phase PACs are often used as static switches for applications like switching on of highly inductive loads without transients or for regulating output AC voltages by switching in tapings of a transformer. Such sequence control PACs while controlling the output voltage also permit improvement of the power factor as seen by the source. Sequence control can be two or multiple phase depending upon the application. Typical load voltage and current waveforms are shown in Fig. 26.8. The outer TRIACs connected to thwe higher voltage leads of the input transformer are triffered at the desired angle α, to realize the required load voltage. Obviously this voltage is greater than that available at the low voltage terminal of the transformer. This device continues conduction into the next half of the supply voltage till the load current falls to zero. The inner TR_2 starts conduction subsequently, requiring a wide pulse or a train of pulses. TR_1 can be however triggered by a single pulse.

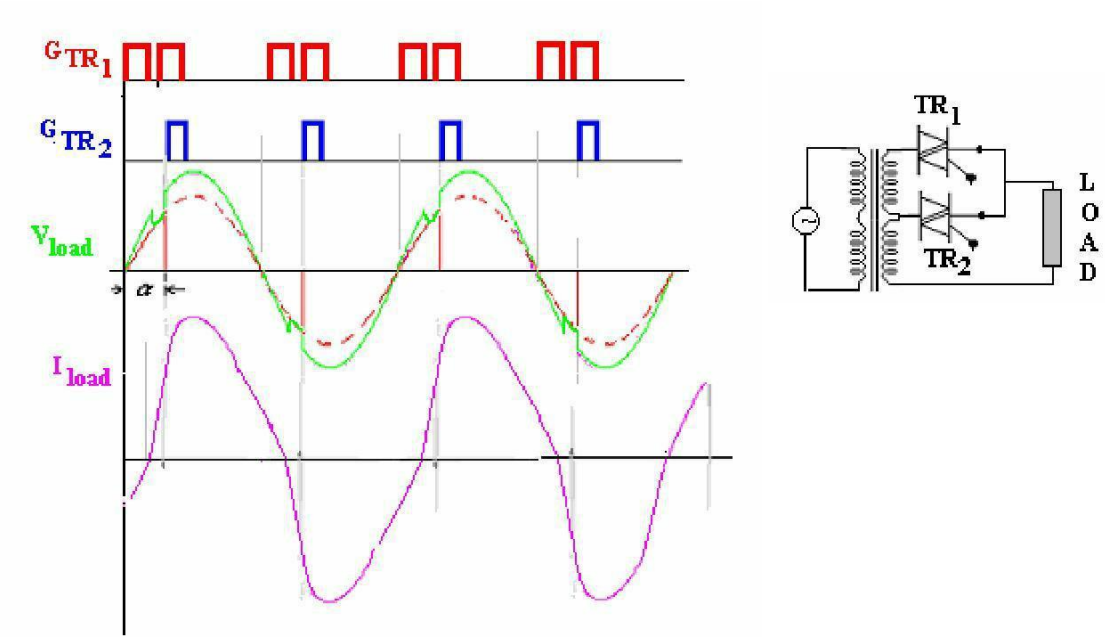


Fig. 26.9 Load voltage and current control with a two-stage sequence control

Practice Questions and Problems with Answers

Q1 A single-phase transformer, assumed to have a negligible resistance compared to its inductance is switched on via a PAC. At what trigger angle will the operation be free from transients?

A1 For the transformer load $\varphi_L \approx 90^o$

Therefore for transient free operation $\alpha = 90^o$

Q2 For the load described in Q1, the PAC is triggered by a single pulse at $\alpha = 60^o$. Sketch the load current waveform.

A2 Since $\alpha < \varphi_L$, the load current should have been continuous. However, the current in the SCR first triggered extinguishes at a β the total load current, $i_L = i_{ss} + i_{tr} = 0$. For this load which can be considered to be highly inductive $\beta \approx 360^o$, say $\approx 360^o$. Thus the first SCR conducts till that angle. The anti-parallel SCR is triggered at $\alpha = 60^o$ corresponding to a $\beta \approx 180 + 60 = 240^o$ when it is still reverse biased. It fails to conduct. The load thus sees only a unipolar current. The load current and voltage waveforms are illustrated in Fig 26. A2. Note that both the load voltage and current waveforms contain DC components.

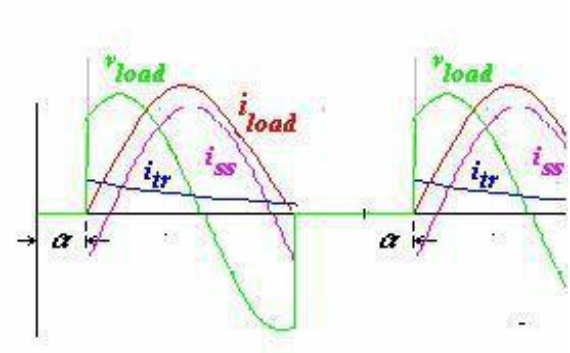


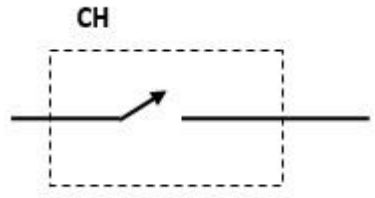
Fig. 26. A2 The load current waveform and its steady-state and transient components when a highly inductive load is switched using single narrow trigger pulses.

Module 5

A chopper uses high speed to connect and disconnect from a source load. A fixed DC voltage is applied intermittently to the source load by continuously triggering the power switch ON/OFF. The period of time for which the power switch stays ON or OFF is referred to as the chopper's ON and OFF state times, respectively.

Choppers are mostly applied in electric cars, conversion of wind and solar energy, and DC motor regulators.

Symbol of a Chopper



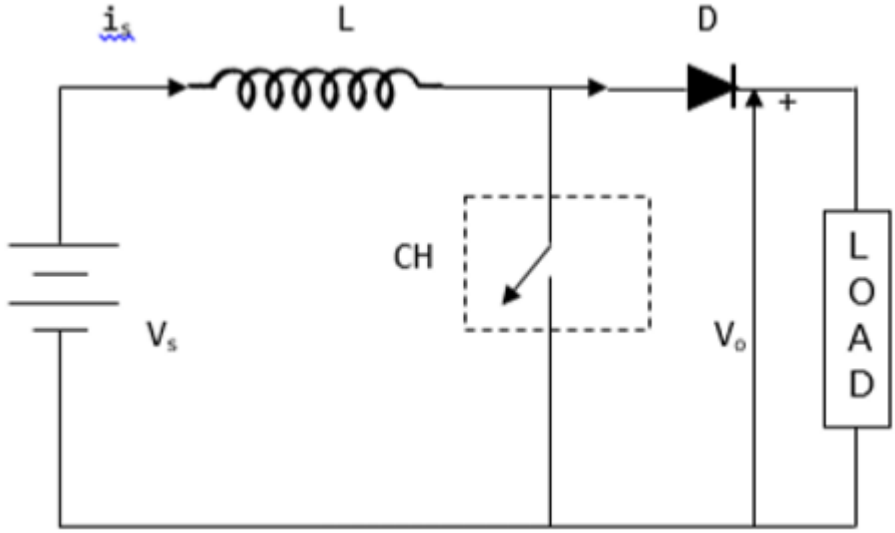
Classification of Choppers

Depending on the voltage output, choppers are classified as –

- Step Up chopper (boost converter)
- Step Down Chopper(Buck converter)
- Step Up/Down Chopper (Buck-boost converter)

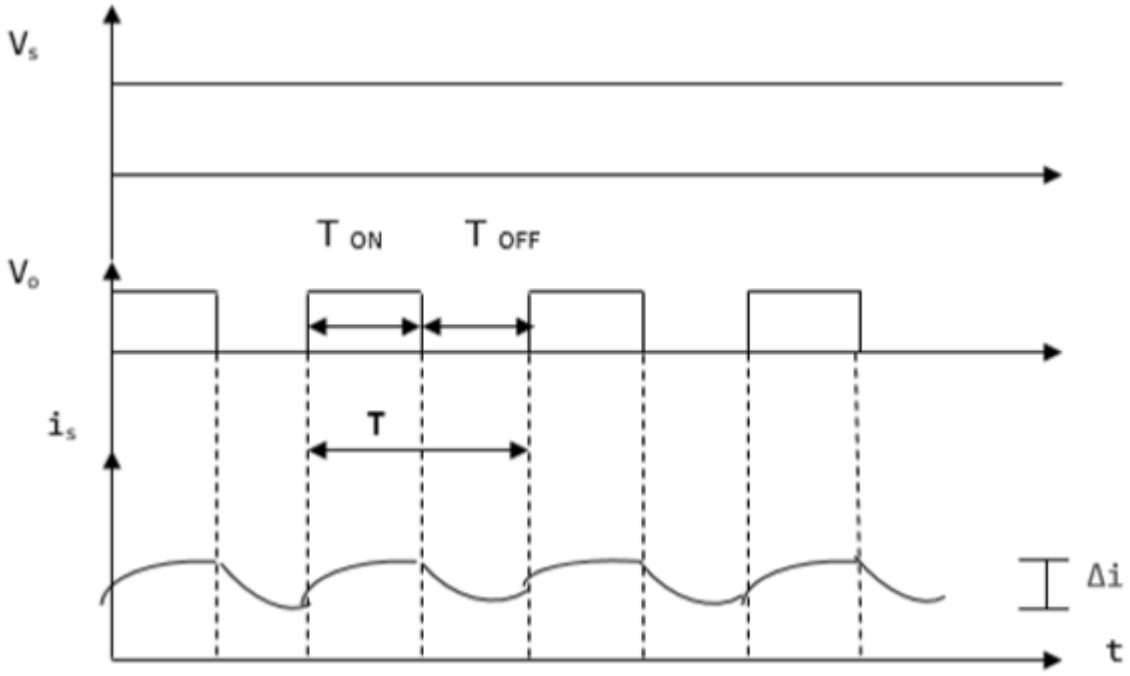
Step Up Chopper

The average voltage output (V_o) in a step up chopper is greater than the voltage input (V_s). The figure below shows a configuration of a step up chopper.



Current and Voltage Waveforms

V_0 (average voltage output) is positive when chopper is switched ON and negative when the chopper is OFF as shown in the waveform below.



Where

T_{ON} – time interval when chopper is ON

T_{OFF} – time interval when chopper is OFF

V_L – Load voltage

V_s – Source voltage

T – Chopping time period = T_{ON} + T_{OFF}

V_o is given by –

$$V0=1T\int TON0VsdtV0=1T\int 0TONVSdt$$

When the chopper (CH) is switched ON, the load is short circuited and, therefore, the voltage output for the period $\mathbf{T_{ON}}$ is zero. In addition, the inductor is charged during this time. This gives $V_S = V_L$

$$Ldidt=VS,Ldidt=VS, \Delta iTON=VSL\Delta iTON=VSL$$

Hence, $\Delta i=VSLTON\Delta i=VSLTON$

Δi = is the inductor peak to peak current. When the chopper (CH) is OFF, discharge occurs through the inductor L. Therefore, the summation of the V_s and V_L is given as follows –

$$V0=VS+VL,VL=V0-VSV0=VS+VL,VL=V0-VS$$

But $Ldidt=V0-VSLdidt=V0-VS$

Thus, $L\Delta iTOFF=V0-VSL\Delta iTOFF=V0-VS$

This gives, $\Delta i=V0-VSLTOFF\Delta i=V0-VSLTOFF$

Equating Δi from ON state to Δi from OFF state gives –

$$VSLTON=V0-VSLTOFFVSLTON=V0-VSLTOFF, VS(TON+TOFF)=V0TOFFVS(TON+TOFF)=V0TOFF$$

$$V0=TVSTOFF=VS(T+TON)TV0=TVSTOFF=VS(T+TON)T$$

This give the average voltage output as,

$$V0=VS1-DV0=VS1-D$$

The above equation shows that V_o can be varied from V_S to infinity. It proves that the output voltage will always be more than the voltage input and hence, it boosts up or increases the voltage level.

Step Down Chopper

This is also known as a buck converter. In this chopper, the average voltage output V_O is less than the input voltage V_S. When the chopper is ON, $V_O = V_S$ and when the chopper is off, $V_O = 0$

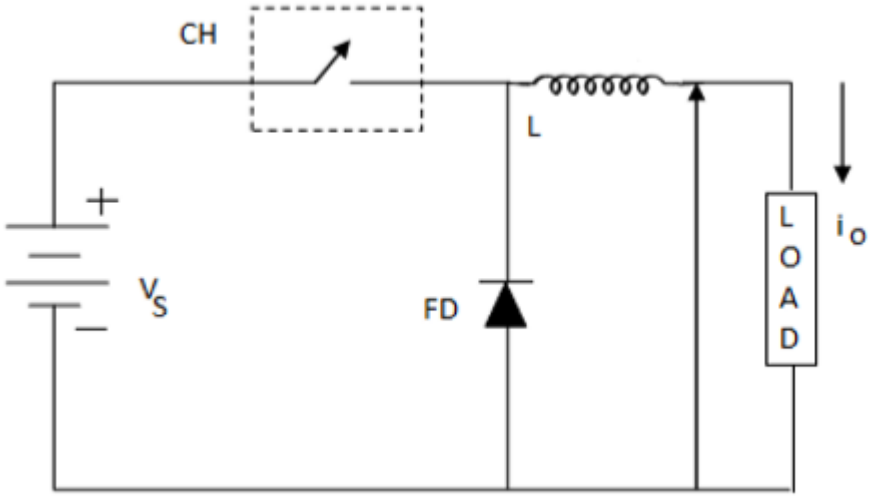
When the chopper is ON –

$V_S=(V_L+V_0), V_L=V_S-V_0, L\frac{di}{dt}=V_S-V_0, L\frac{\Delta i}{T_{ON}}=V_s+V_0$VS=(VL+V0),VL=VS−V0,Ldidt=VS−V0,LΔiTON=Vs+V0

Thus, peak-to-peak current load is given by,

$\Delta i=\frac{V_s-V_0}{L}T_{ON}$Δi=Vs−V0LTON

Circuit Diagram



Where **FD** is free-wheel diode.

When the chopper is OFF, polarity reversal and discharging occurs at the inductor. The current passes through the free-wheel diode and the inductor to the load. This gives,

$L\frac{di}{dt}=V_0$.....(i)Ldidt=V0.....(i)

Rewritten as $-L\frac{\Delta i}{T_{OFF}}=V_0$L**Δ**iTOFF=V0

$\Delta i=\frac{V_0}{T_{OFF}}L$.....(ii)Δi=V0TOFFL.....(ii)

Equating equations (i) and (ii) gives;

$V_S-V_0L T_{ON}=V_0L T_{OFF}$VS−V0LTON=V0LTOFF

$V_S-V_0V_0=T_{OFF}T_{ON}$VS−V0V0=TOFFTON

$V_SV_0=T_{ON}-T_{OFF}T_{ON}$VSV0=TON−TOFFTON

The above equation gives;

$V_0=T_{ON}TV_S=DV_SV0=TONTVS=DVS$

Equation (i) gives –

$\Delta i=\frac{V_S-DV_S}{L}DT$Δi=VS−DVSLDT, from $D=\frac{T_{ON}}{T}$D=TONT

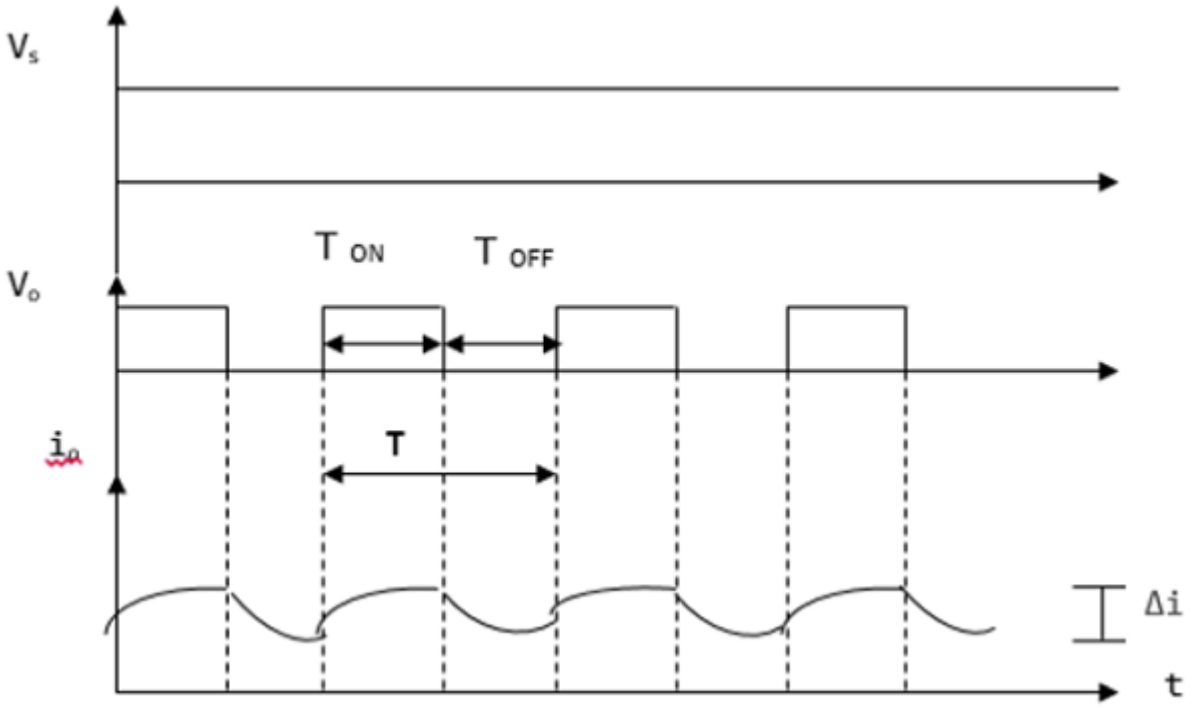
$=V_S-(1-D)DLf$=VS−(1−D)DLf

$f=\frac{1}{T}=f=1T=$chopping frequency

Current and Voltage Waveforms

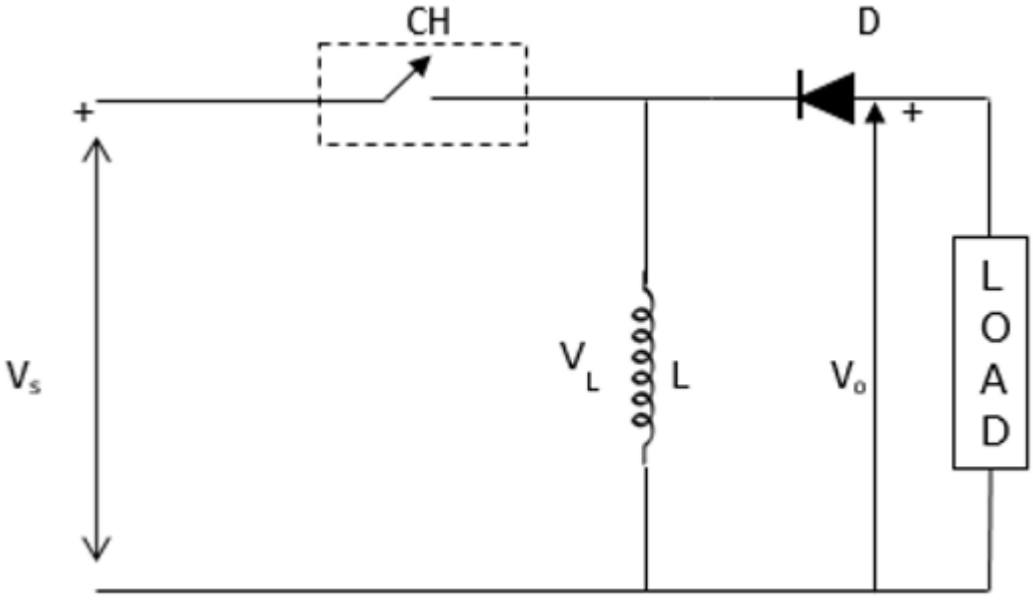
The current and voltage waveforms are given below –

For a step down chopper the voltage output is always less than the voltage input. This is shown by the waveform below.



Step Up/ Step Down Chopper

This is also known as a buck-boost converter. It makes it possible to increase or reduce the voltage input level. The diagram below shows a buck-boost chopper.



When the chopper is switched ON, the inductor L becomes charged by the source voltage V_s. Therefore, $V_s = V_L$.

$$L\frac{di}{dt}=V_S \quad L\frac{di}{dt}=V_S$$

$$\Delta i=\frac{V_S}{L}T_{ON}=\frac{V_S}{LT}T_{ON}T=DV_SLf \quad \Delta i=\frac{V_S}{L}T_{ON}=\frac{V_S}{LTT}T_{ON}T=DV_SLf$$

Because –

$D=T_{ON}TD=TONT$ and $f=1T$.....(iii)$f=1T$.....
.(iii)

When the chopper is switched OFF, the inductor's polarity reverses and this causes it to discharge through the diode and the load.

Hence,

$$V_0=-V_LV0=-VL$$
$$Ldidt=-V_0Ldidt=-V0$$

$L\Delta i_{OFF}=-V_0L\Delta iTOFF=-V0$,
thus $\Delta i=-V_0LT_{OFF}$.....(iv)$\Delta i=-V0LTOFF$.....(iv)
Evaluating equation (iii) and (iv) gives –

$DV_SLf=-V_0LT_{OFF}DVSLf=-V0LTOFF$, $DV_S=-DV_S=-V_0T_{OFF}fDVS=-DVS=-V0TOFFf$
$DV_S=-V_0T-T_{ON}T=-V_0(1-T_{ON}T)DVS=-V0T-TONT=-V0(1-TONT)$, $V_0=-DV_S1-DV0=-DVS1-D$
Because $D=T_{ON}T=T-T_{OFF}1-DD=TONT=T-TOFF1-D$
This gives,

$V_0=DV_S1-DV0=DVS1-D$
D can be varied from 0 to 1. When, D = 0; V_o = 0

When D = 0.5, $V_o = V_s$

When, D = 1, $V_o = \infty$.

Hence, in the interval $0 \le D \le 0.5$, output voltage varies in the range $0 \le V_o < V_s$ and we get step down or Buck operation. Whereas, in the interval $0.5 \le D \le 1$, output voltage varies in the range $V_s \le V_o \le \infty$ and we get step up or Boost operation

Single Phase Inverter

There are two types of single phase inverters – full bridge inverter and half bridge inverter.

Half Bridge Inverter

This type of inverter is the basic building block of a full bridge inverter. It contains two switches and each of its capacitors has a voltage output equal to $V_{dc}2Vdc2$. In addition, the switches complement each other, that is, if one is switched ON the other one goes OFF.

Full Bridge Inverter

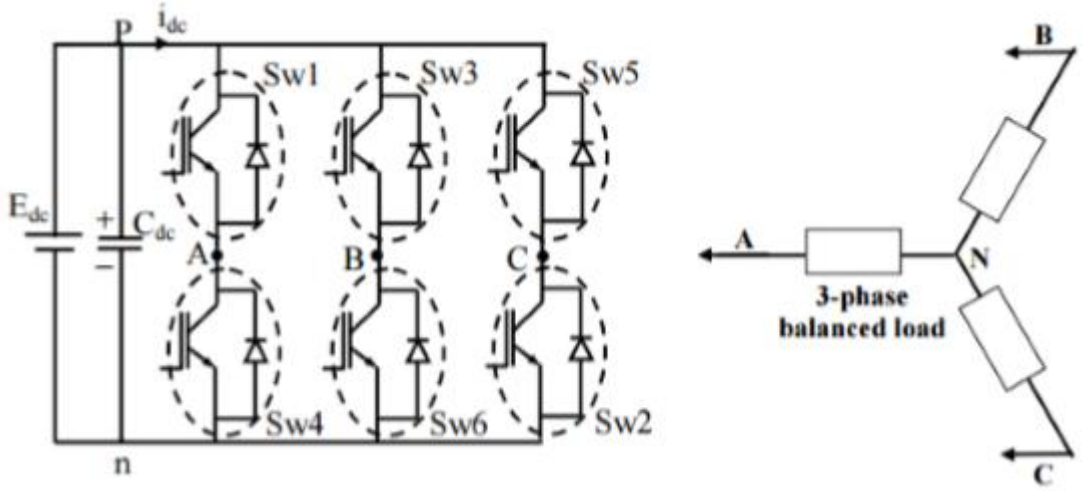
This inverter circuit converts DC to AC. It achieves this by closing and opening the switches in the right sequence. It has four different operating states which are based on which switches are closed.

Three Phase Inverter

A three-phase inverter converts a DC input into a three-phase AC output. Its three arms are normally delayed by an angle of 120° so as to generate a three-phase AC supply. The inverter switches each has a ratio of 50% and

switching occurs after every T/6 of the time T (60° angle interval). The switches S1 and S4, the switches S2 and S5 and switches S3 and S6 complement each other.

The figure below shows a circuit for a three phase inverter. It is nothing but three single phase inverters put across the same DC source. The pole voltages in a three phase inverter are equal to the pole voltages in single phase half bridge inverter.

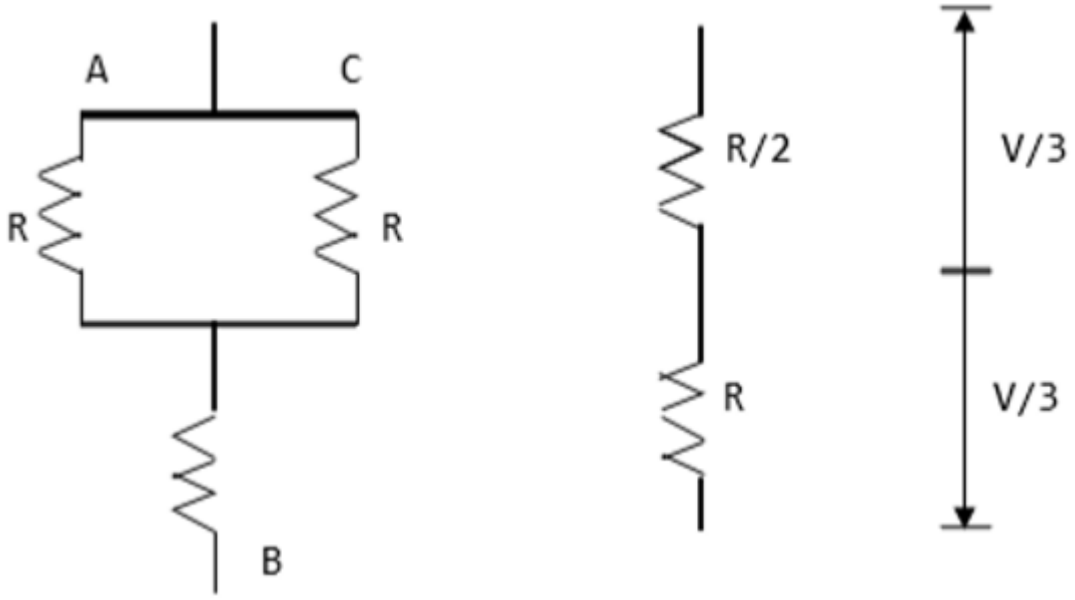


The two types of inverters above have two modes of conduction – **180° mode of conduction** and **120° mode of conduction**.

180° mode of conduction

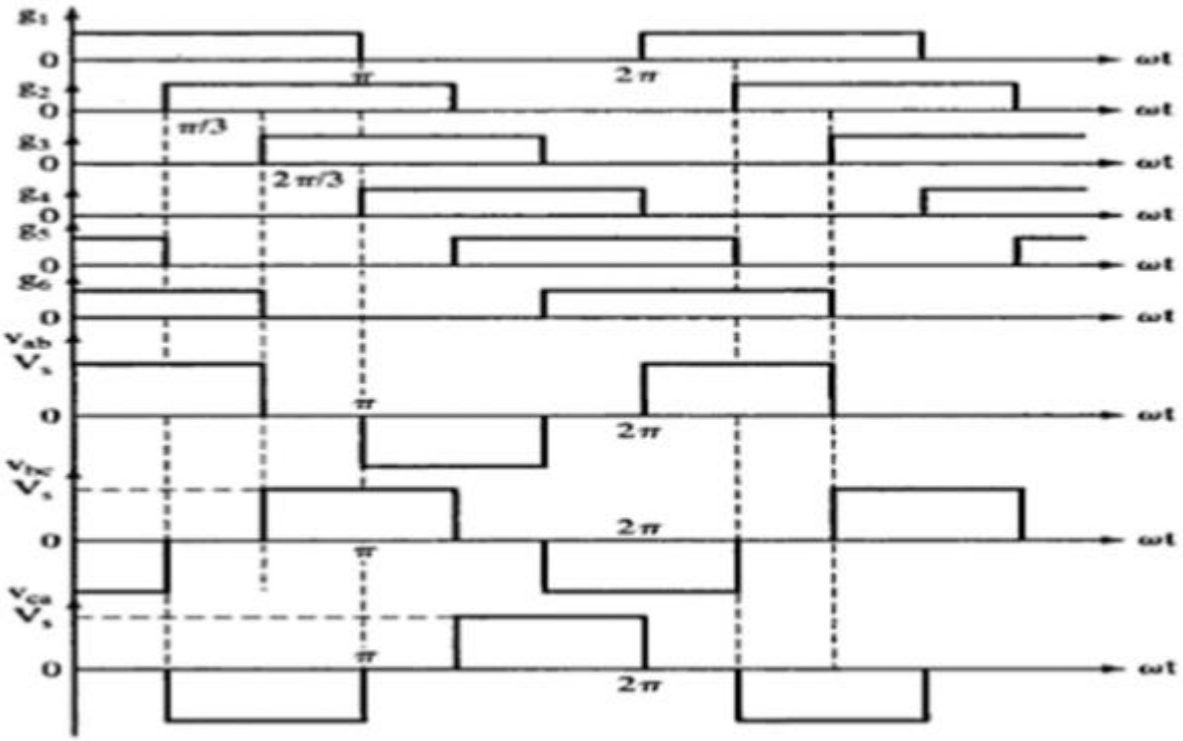
In this mode of conduction, every device is in conduction state for 180° where they are switched ON at 60° intervals. The terminals A, B and C are the output terminals of the bridge that are connected to the three-phase delta or star connection of the load.

The operation of a balanced star connected load is explained in the diagram below. For the period 0° – 60° the points S1, S5 and S6 are in conduction mode. The terminals A and C of the load are connected to the source at its positive point. The terminal B is connected to the source at its negative point. In addition, resistances R/2 is between the neutral and the positive end while resistance R is between the neutral and the negative terminal.



The load voltages are gives as follows; $V_{AN} = V/3$, $V_{BN} = -2V/3$, $V_{CN} = V/3$	The line voltages are given as follows; $V_{AB} = V_{AN} - V_{BN} = V$, $V_{BC} = V_{BN} - V_{CN} = -V$, $V_{CA} = V_{CN} - V_{AN} = 0$

Waveforms for 180° mode of conduction



Current Source Inverter (CSI) – A current source inverter is supplied with a variable current from a DC source that has high impedance. The resulting current waves are not influenced by the load.